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# THESIS

**THE VLSI IMPLEMENTATION OF A GIC SWITCHED CAPACITOR FILTER**

by

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March 1998

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# THE VLSI IMPLEMENTATION OF A GIC SWITCHED CAPACITOR FILTER


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## ABSTRACT

In this research, the design and VLSI implementation of a digitally programmable active analog filter, based on the Generalized Immittance Converter (GIC) circuit, are presented. The programmable features include the filter type (band-pass, high-pass, low-pass or notch), the center or cut-off frequency, and the quality factor. Switched capacitor networks are used to implement resistances. The design was first simulated and then implemented on a wire-wrap board and tested. The circuit was then modeled and re-simulated using the Cadence Design Tools software package. Once the modeled circuit passes all design rule checks the final chip design was then submitted for fabrication. This research project will help provide a knowledge base for using Cadence software for VLSI CMOS design. Once the chip has been fabricated and tested it will provide a base for further development of stray insensitive VLSI design of analog circuits.

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# I. INTRODUCTION

## A. BACKGROUND

In the 1960's most electrical circuits and systems were designed and implemented using analog devices such as communications filters. As circuit technology has progressed through the 70's and 80's, new design alternatives are available to practicing engineers. In particular, significant advances have been made in the development of digital components, making them smaller, lighter and faster than their analog counterparts. As a result of this reduction in size and improved speed, many applications were being converted from analog technology to digital. Now in the 1990's digital circuits are capable of performing even more complex functions. For example, digital filters now routinely replace analog filters in a variety of circuits.

Establishing the proper interface between very complex digital circuits and analog circuits is critical to developing the systems required in today's world marketplace. In particular, analog circuits are still vital in a variety of applications including spacecraft control, remote sensing, and communications equipment. In the past, interfacing an analog system to a digital system was normally accomplished by separate components. Now it is possible to integrate the interface into the design of the digital component. By integrating the analog interface, circuit size and weight are minimized.

Very Large Scale Integration (VLSI) techniques provide the capability to integrate analog and digital circuits on the same microchip. High-power Computer Aided Design (CAD) tools and simulation models are tools readily available to the designer of VLSI components. By using these tools, it is possible to design high performance inexpensive interface technology. For instance, a circuit designer can develop and build a programmable stray insensitive mixed-

signal (Digital/Analog) VLSI filter on a single microchip. The research work presented in this thesis reports on the design of a stray insensitive Programmable General Immittance Converter (GIC) circuit using the Cadence VLSI Complementary Metal Oxide Semiconductor (CMOS) design package. [1]

## B. THESIS ORGANIZATION

The goal of this thesis is to design, manufacture and test a digitally programmable stray insensitive GIC filter. Basic filter structures and the reasons for choosing the GIC design are discussed in Chapter II. In Chapter III the advantages and operation of switched capacitor filters are explained. Chapter IV examines the operational amplifier and provides test results to validate the applicability of its application in the GIC filter design. Chapter V details the design and testing of a digitally programmable GIC filter. Design limitations and VLSI layout of the GIC filter are documented in Chapter VI. Finally, conclusions and recommendations for future work are outlined in Chapter VII.

# II. THE PROGRAMMABLE GENERALIZED IMMITTANCE CONVERTER DEVELOPMENT

## A. BASIC FILTERS

A filter is a device that consists of a group of components including resistors, capacitors, inductors and sometimes active devices such as operational amplifiers. The primary purpose of most filters is to modify the amplitude response of a circuit to a signal so that certain frequencies are attenuated or blocked, while others pass through unchanged. Most filters are placed in a group based on frequency ranges that are attenuated or passed. According to this classification, there emerge four basic filter topologies whose ideal frequency response characteristics are described in Table 2.1. These include low-pass, high-pass, band-pass and notch filters. For instance, a low-pass filter is one that attenuates the high-frequency components of a signal while passing through the low-frequency components

A circuit designer attempts to implement an approximation to the ideal characteristics illustrated in Table 2.1. An ideal filter would pass only the desired frequencies and attenuate all others. In order to achieve near ideal filter response, the filter circuit generally becomes more complex, contains more components and is more expensive. With this background in mind, the variation in the quality of each component will have to be examined.

The Quality factor, or "Q", is a parameter used to describe the selectivity performance of a filter. For a first order filter, the Q parameter relates the distance of the filter pole to the $j\omega-axis$. For a more selective filter the Q value must be high. A high Q implies that the poles

| RC Low-Pass Filter | Ideal Response |
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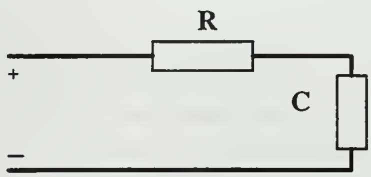
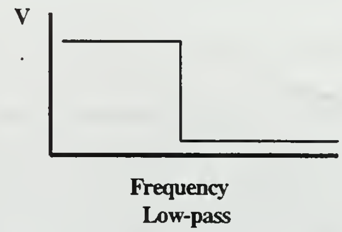
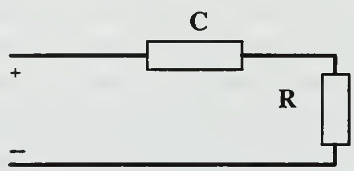
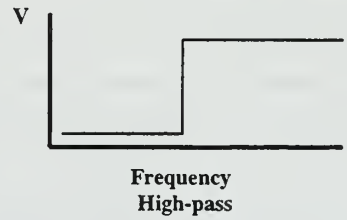
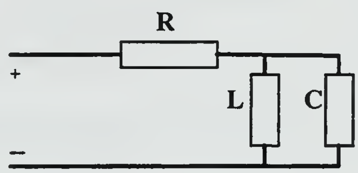
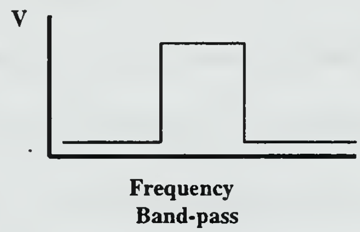
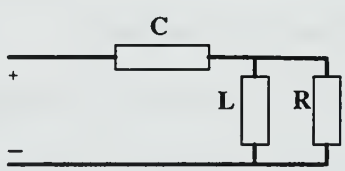
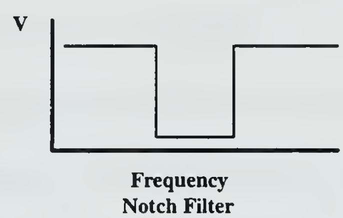
|  |  |
| **RC High-Pass Filter** | **Ideal Response** |
|  |  |
| **RLC Band-Pass Filter** | **Ideal Response** |
|  |  |
| **RLC Notch Filter** | **Ideal Response** |
|  |  |

Table 2.1: Four Basic Filters with Frequency Response

of the filter have to be closer to the $j\omega - axis$. The Q of a filter can be calculated by taking the inverse of the normalized bandwidth of the filter. Calculations for the normalization can be achieved by using the half power (3dB) point of the filter. Figure 2.1 illustrates the Q calculation. [2]

$$Q = \frac{\omega_0}{\omega_1 - \omega_2} \qquad \text{(Eq. 2.1)}$$

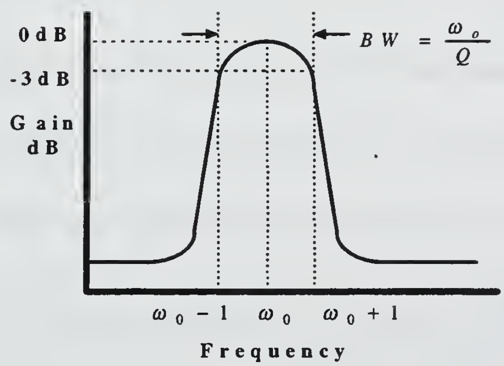



**Figure 2.1: Q Factor for Band-Pass Filter**

Filters are designed to accept or reject a frequency or range of frequencies. Typically the filter is described mathematically in the frequency domain through the use of transfer functions. The order of the denominator polynomial of the transfer function determines the order of the filter. The second-order bi-quad transfer functions are considered to be the basic building blocks for filters. Transfer functions for the four basic filter structures are presented in Table 2.2. The designer may choose a higher order filter but the complexity of the system would increase since realization would require additional components. [3]

| Filter Topology | Transfer Function |
|---|---|
| Low-pass | $H(s)=\dfrac{2\omega_p^2}{s^2+\dfrac{\omega_p}{Q_p}s+\omega}$ |
| High-pass | $H(s)=\dfrac{2s^2}{s^2+\dfrac{\omega_p}{Q_p}s+\omega}$ |
| Band-pass | $H(s)=\dfrac{\dfrac{2\omega_p}{Q_p}s}{s^2+\dfrac{\omega_p}{Q_p}s+\omega}$ |
| Notch | $H(s)=\dfrac{s^2+\omega_n^2}{s^2+\dfrac{\omega_p}{Q_p}s+\omega}$ |

**Table 2.2: Four Filter Topologies with Corresponding Transfer Functions**

## B. PASSIVE AND ACTIVE FILTERS

Prior to advances in solid-state technology, inductors and capacitors were used exclusively for realizing simple filters. These components proved to be effective for realizing low-pass, high-pass, band-pass, and notch filters. These passive LC circuits normally work well at high frequencies, but LC circuits have very poor performance at low frequencies. Inductors are not practical for low frequency applications because of the required large size and non-ideal characteristics. Therefore, considerable interest has been placed on designing inductorless filters. The operational amplifier (OP AMP) is the major component in inductorless filter design.

OP AMPs, resistors and capacitors are the major components of an active-RC filter (inductorless filter circuit). The basic idea is to realize, using feedback techniques, transfer functions previously only attainable using both inductors and capacitors. This design can also be implemented using switched capacitor technologies. Many different circuits have been designed to realize an inductorless filter. However, the GIC filter is the least sensitive to the non-ideal characteristics of the operational amplifier. [4]

### C. THE GIC FILTER

Filters are designed in various configurations. The most popular configurations include the Bessel-Thompson, Chebyshev, and Butterworth filters. Engineers like to exploit certain characteristics, like filter sensitivities, for specific applications. Performance may be viewed in terms of sensitivity. The variation of components with temperature, fabrication process and parasitic capacitance will all effect the filter performance. Sensitivity calculations should be compared to actual operating parameters of a comparable filter design. Sensitivity calculations are used when optimizing a filter design. A detailed calculation of sensitivity for a highpass filter, as an example, will be covered later in this chapter.

A well known circuit that is very tolerant to the non-ideal operational amplifier characteristics is the Generalized Impedance Converter introduced by Antoniou [4]. The GIC filter design is based on the properties of Antoniou's Generalized Impedance Converter. The GIC filter design was introduced by Mikhael and Bhattachararyya [4] and proved to be very insensitive to non-ideal component characteristics and variations in component values. Figure 2.2 shows the general topology of the GIC filter.

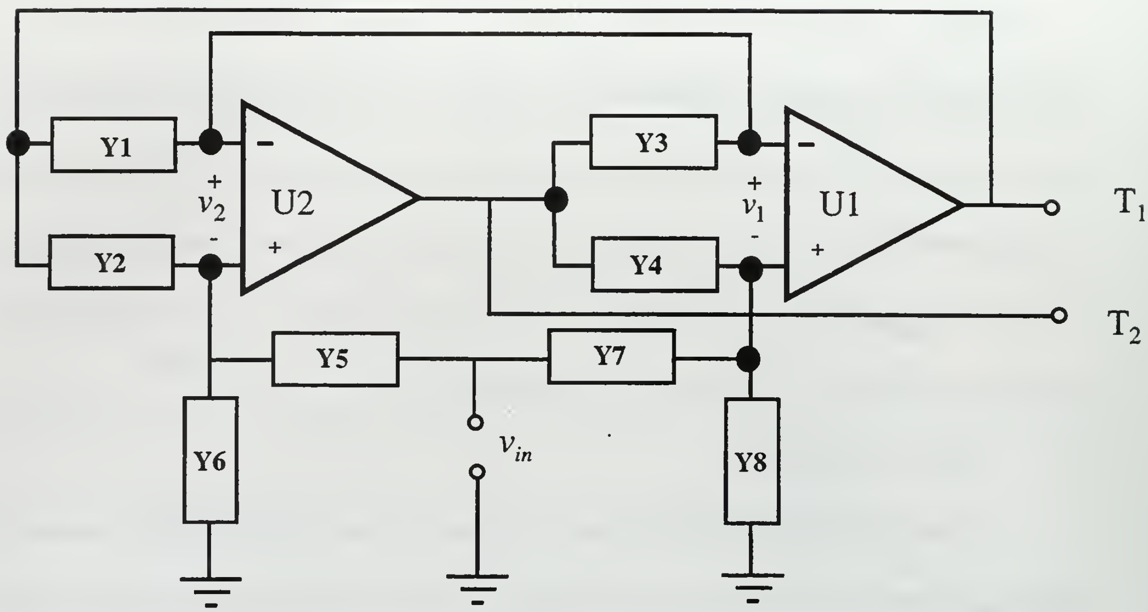



**Figure 2.2: Generalized Immittance Converter Filter Topology**

The transfer functions relating $v_{in}$ to voltages $v_1$ and $v_2$ are given by

$$T_1 = \frac{v_1}{v_{in}} = \frac{Y1Y4Y5 + Y3Y7(Y2 + Y6) - Y3Y5Y8}{Y1Y4(Y5 + Y6) + Y2Y3(Y7 + Y8)} \quad \text{(Eq. 2.2)}$$

$$T_2 = \frac{v_2}{v_{in}} = \frac{Y1Y4Y5 + Y1Y5Y8Y + Y2Y3Y7 - Y1Y6Y7}{Y1Y4(Y5 + Y6) + Y2Y3(Y7 + Y8)} \quad \text{(Eq. 2.3)}$$

| Filter Type | Y1 | Y2 | Y3 | Y4 | Y5 | Y6 | Y7 | Y8 |
|---|---|---|---|---|---|---|---|---|
| Lowpass | G | C | C+G/QP | G | G | 0 | O | G |
| Highpass | G | G | C | G | 0 | G | C | G/QP |
| Bandpass | G | G | C | G | 0 | G | G/QP | C |
| Notch | G | G | C | G | G | 0 | C | G/QP |

**Table 2.3: GIC Filter Admittance Values**

From the admittance values listed in Table 2.3, the filter topologies depicted in Table 2.1 can be realized. The outputs for the low-pass and notch filter topologies are taken from $T_1$, while the outputs for the high-pass and band-pass topologies are taken from $T_2$. Nodal analysis can be used to derive the transfer functions for each filter with the outputs taken from $T_1$ or $T_2$. In the previous transfer functions (Equations 2.2 and 2.3), operational amplifiers were assumed to be ideal in order to simplify the derivation of the GIC filter equations. Comparing the equations for $T_1$ for both the ideal and non-ideal case, we can be shown that the difference between the two frequency response plots is very small (Figure 2.3a and 2.3b). As a result of this excellent sensitivity property, the GIC filter is used in this research. Figure 2.4 demonstrates the four different topologies.

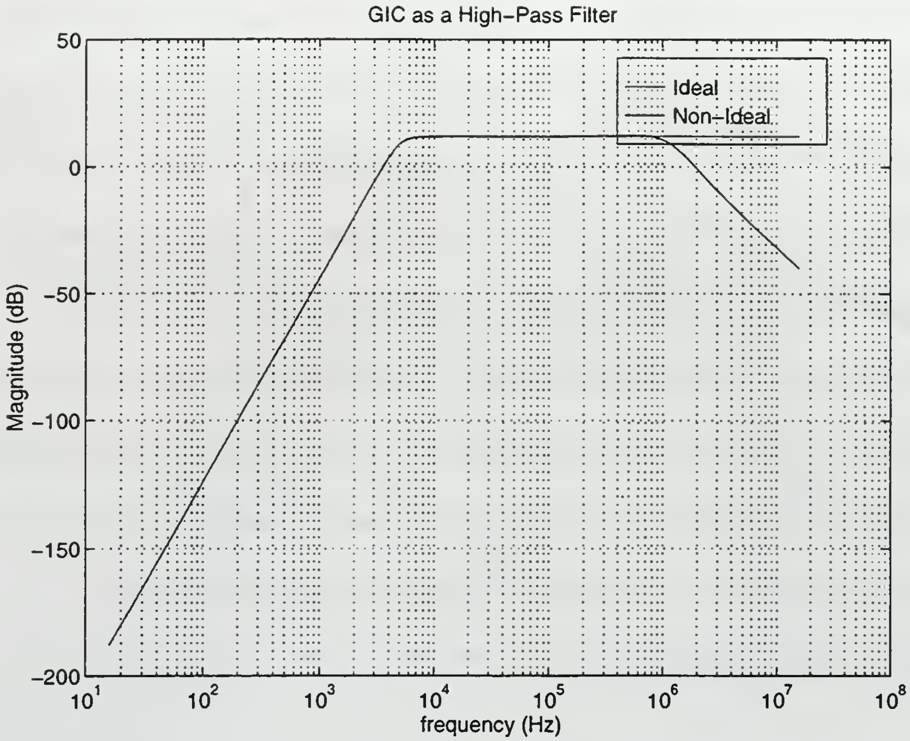



**Figure 2.3a: Ideal vs Non-Ideal Frequency Response**

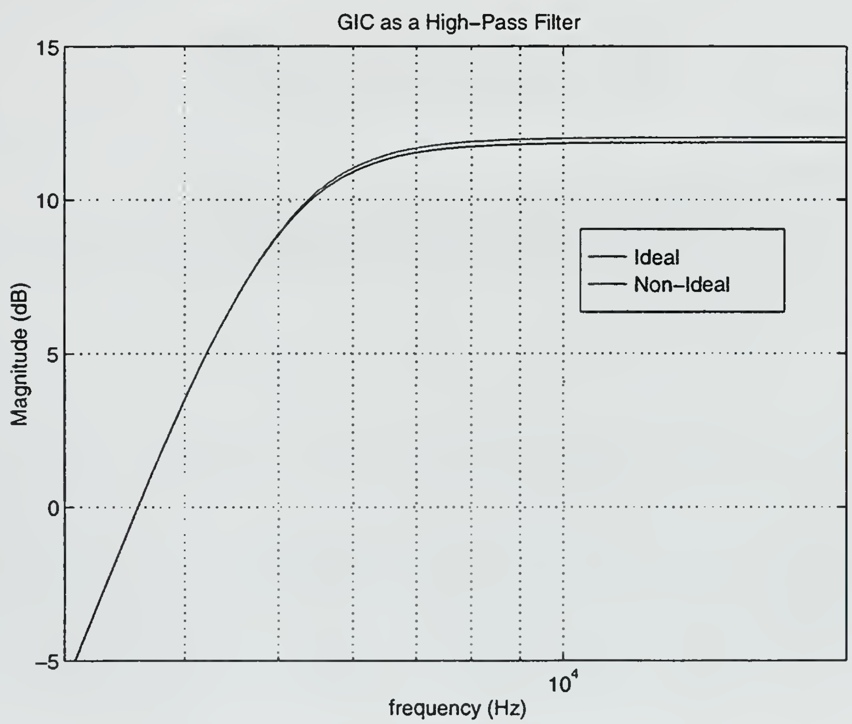



**Figure 2.3b: Magnified Frequency Response Comparison**

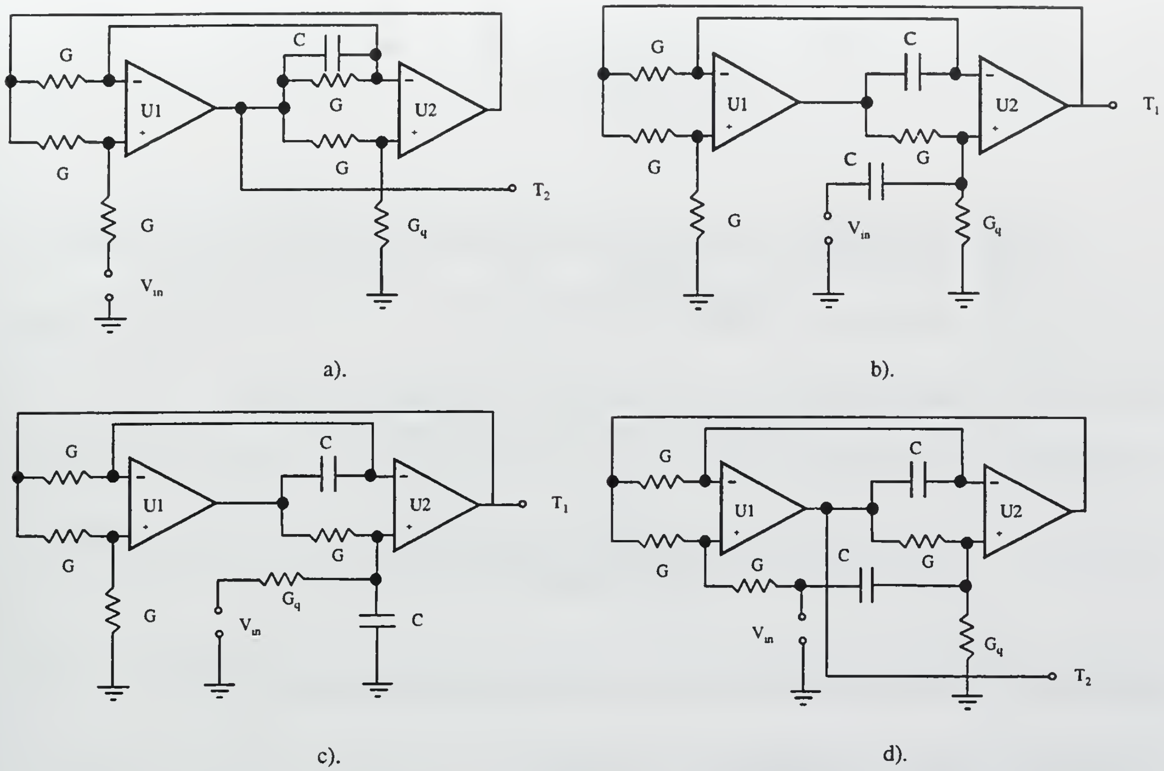



**Figure 2.4: Four Topologies of the GIC Filter: a.) Low-Pass Filter, b.) High-Pass Filter c.) Band-Pass Filter, d.) Notch Filter**

## D. SENSITIVITY

Since component values vary, the actual response of the filter deviates from the ideal. In order to quantify and predict the deviations of the filter, the designer must examine the sensitivity of the circuit. Component sensitivity can be calculated by using the classical sensitivity function

$$S_x^y = \underset{\Delta X \to 0}{LIM} \frac{\Delta y/y}{\Delta x/x} = \frac{\partial y}{\partial x}\frac{x}{y} \qquad \text{(Eq. 2.4)}$$

where $x$ represents the resistor, capacitor or Gain Band-Width-Product of the operational amplifier and $y$ represents the parameter of interest such as $\omega_0$ or $Q$. For example (Eq. 2.5) and (Eq. 2.6), show the non-ideal sensitivity results for a high-pass filter [5]:

$$\int_{G2}^{W_O} = \int_{C3}^{W_O} = \int_{C7}^{W_O} = \frac{C7}{W_O}\frac{\partial W_O}{\partial C7} = \frac{C7V7^{\frac{1}{2}}}{\sqrt[4]{\dfrac{G1^2G4^2G6^2}{G2^2C3^2}}}\left(-\frac{1}{2}\right)C7^{-\frac{3}{2}}\sqrt{\frac{G1^2G4^2G6}{G2^2C3^2}} = -\frac{1}{2} \qquad \text{(Eq. 2.5)}$$

$$\int_{G1}^{W_O} = \int_{G4}^{W_O} = \int_{G6}^{W_O} = \frac{G6}{W_O}\frac{\partial W_O}{\partial G6} = \frac{G6G6^{\frac{1}{2}}}{\sqrt[4]{\dfrac{G1^2G4^2}{G2^2C3^2C7^2}}}\left(\frac{1}{2}\right)G6^{-\frac{3}{2}}\sqrt{\frac{G1^2G4^2}{G2^2C3^2C7^2}} = \frac{1}{2} \qquad \text{(Eq. 2.6)}$$

One can also calculate the passive sensitivity using the ideal transfer function:

$$T_1 = \frac{2s^2}{s^2 + \dfrac{\omega_p}{Q_p}s + (\omega_p)^2} \qquad \text{(Eq. 2.7)}$$

By cascading two GIC filters, a 4th-order filter can be realized. By using (Eq. 2.7), the sensitivities for such a 4th-order filter can be calculated:

$$\int_{G2}^{W_O} = \int_{C3}^{W_O} = \int_{C7}^{W_O} = \frac{C7}{W_O}\frac{\partial W_O}{\partial C7} = \frac{C7}{\sqrt[4]{\dfrac{G1G4G6}{G2C3}}}\left(-\frac{1}{4}\right)C7^{-\frac{3}{4}}\sqrt{\frac{G1G4G6}{G2C3}}$$

$$= \frac{C7}{\sqrt{\dfrac{1}{C7}}}^{-\frac{1}{2}} C7^{-\frac{3}{4}} = -\tfrac{1}{4} \qquad \text{(Eq. 2.8)}$$

$$\int_{G1}^{W_O} = \int_{G4}^{W_O} = \int_{G6}^{W_O} = \frac{G1}{W_O}\frac{\partial W_O}{\partial G1} = \frac{G1}{\sqrt[4]{\dfrac{G1G4G6}{G2C3C7}}}\left(\frac{1}{4}\right)G1^{-\frac{1}{4}}\sqrt{\frac{G4G6}{G2C3C7}}$$

$$= G1\,\tfrac{1}{4}\frac{G1^{-\frac{1}{4}}}{\sqrt[4]{G1}} = \tfrac{1}{4} \qquad \text{(Eq. 2.9)}$$

$$\int_{G8}^{W_O} = \frac{G8}{\left(G8\dfrac{C7}{QP}\right)}\frac{C7}{QP}G8^{0} = 1 \qquad \text{(Eq. 2.10)}$$

The previous method illustrates analytical calculations of GIC filter sensitivities. A graphical method may also be used. Using the GIC non-ideal transfer function (Eq. 2.11)

$$T_2 = \frac{((Y7\,Y1 + Y3)(Y2 + Y5 + Y6)(1/A1)) + ((Y1\,Y4\,Y5) +}{((Y2 + Y5 + Y6)(Y4 + Y7 + Y8)(Y1 + Y3)(1/(A1A2))) + Y1(Y2 + Y5 + Y6)(Y4 + Y7 + Y8)(1/A1)) +} \cdots$$

$$\cdots \frac{(Y3\,Y7(Y2 + Y6)) - Y3\,Y5\,Y8))}{(Y3(Y2 + Y5 + Y6)(Y4 + Y7 + Y8)(1/A2)) + (Y1Y4(Y5 + Y6)) + (Y2Y3(Y7 + Y8))} \qquad \text{(Eq. 2.11)}$$

where $A1 = A2 = \dfrac{\omega t}{s}$, and varying each of the filter components listed in Figure 5 by ten percent, we obtain the transfer function frequency response which is illustrated in Figures 2.6 through 2.13. A MATLAB program, is used to calculate the sensitivity for a 4th-order high-pass filter while varying eight different component values by ± 10%. The MATLAB program outputs two graphs (graph 1 depicts filter response of filter and graph 2 is the magnification of graph 1) per component depicting variations in sensitivity. Figure 2.6a and 2.6b show the

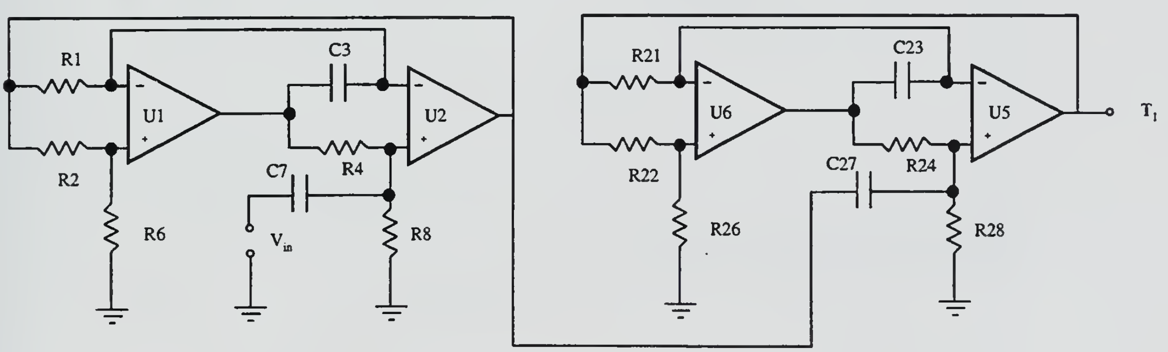



**Figure 2.5: 4th Order High Pass filter**

effects of an increase or decrease of 10% on R2. Upon comparing these frequency response plots to those in Figure 2.7 through 2.13, it is clear that variations in the R2 component has the largest impact on the magnitude response.

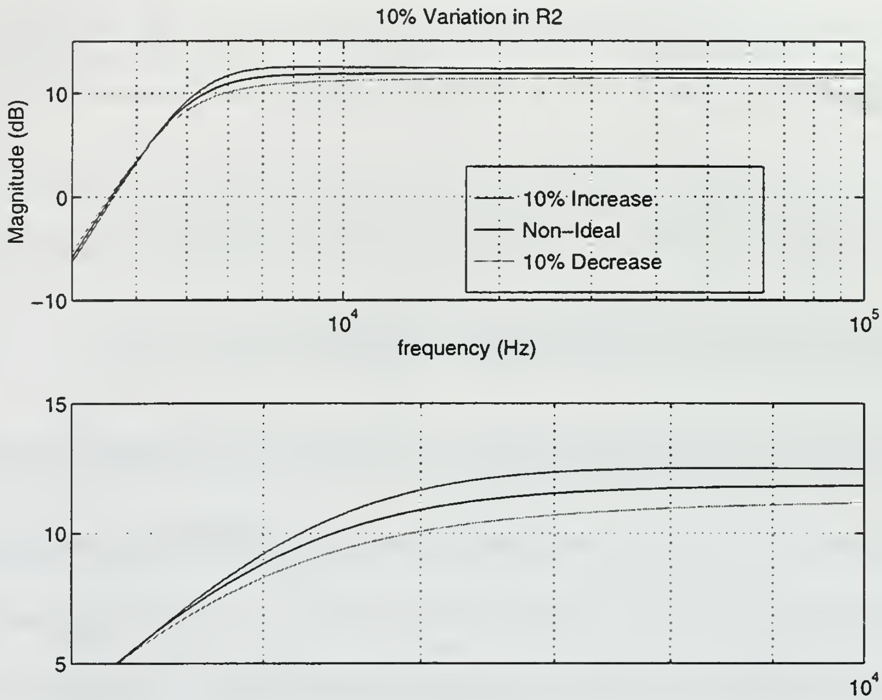



**Figure 2.6: a) 10% Variation in R2 b) Magnified 10% Variation in R2**

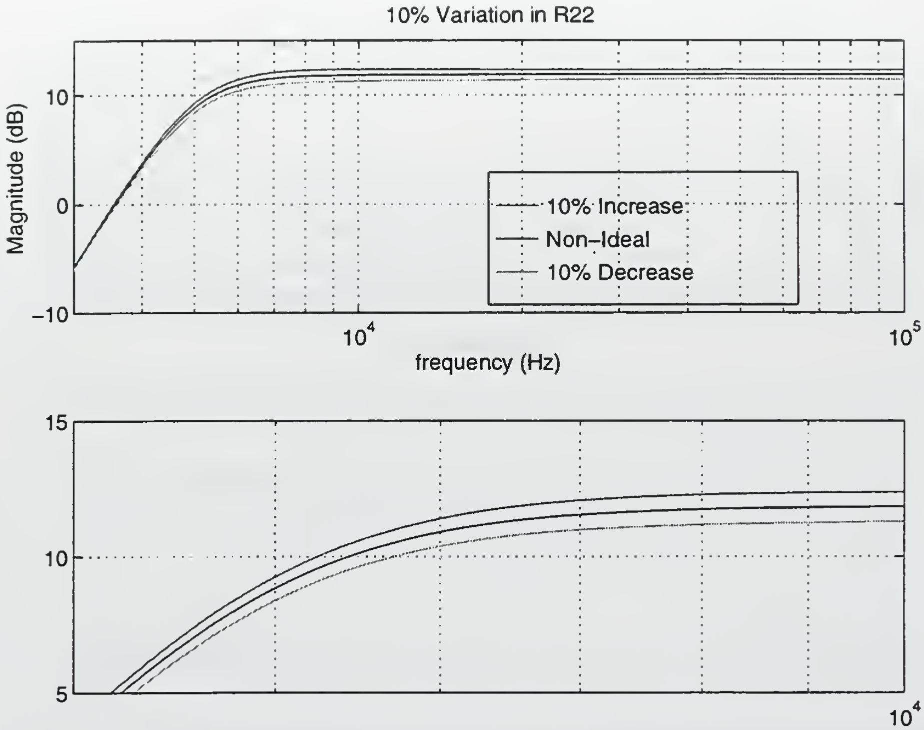



Figure 2.7: a) 10% Variation in R22 b) Magnified 10% Variation in R22

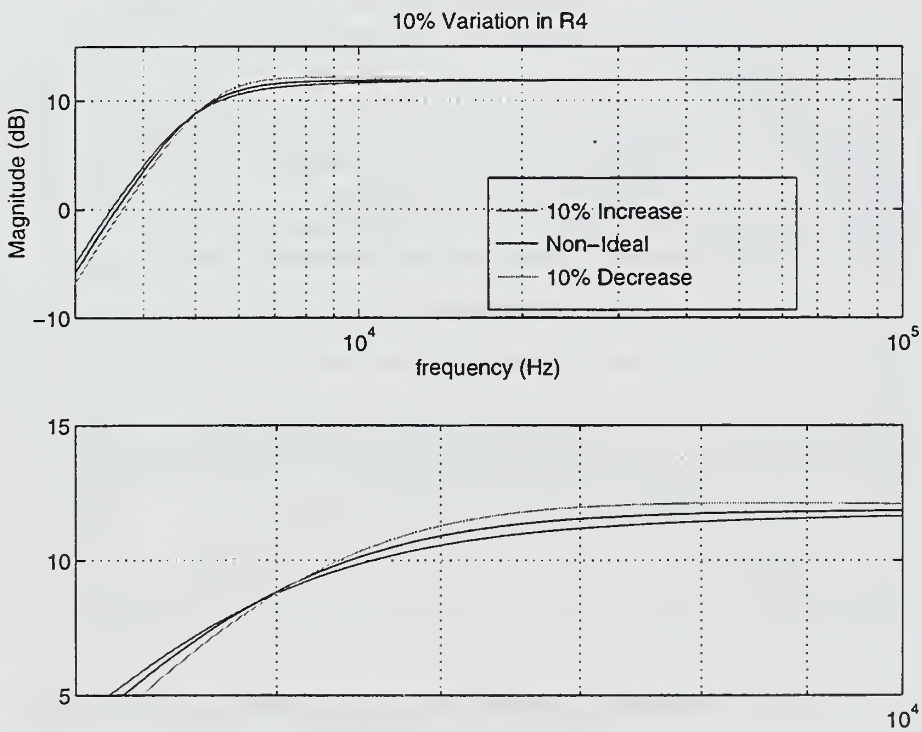



Figure 2.8: a) 10% Variation in R4 b) Magnified 10% Variation in R4

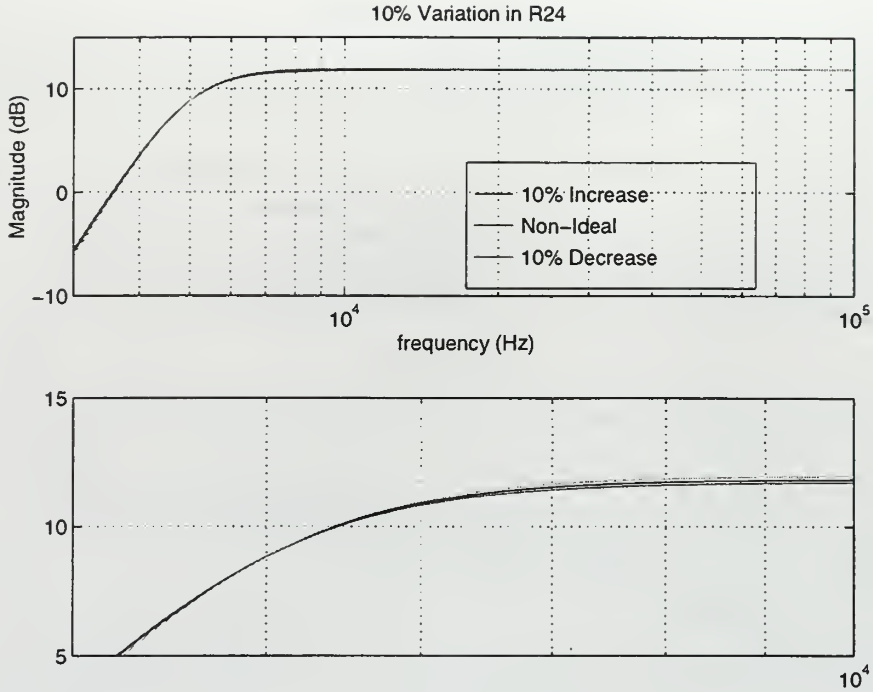



Figure 2.9: a) 10% Variation in R24 b) Magnified 10% Variation in R24

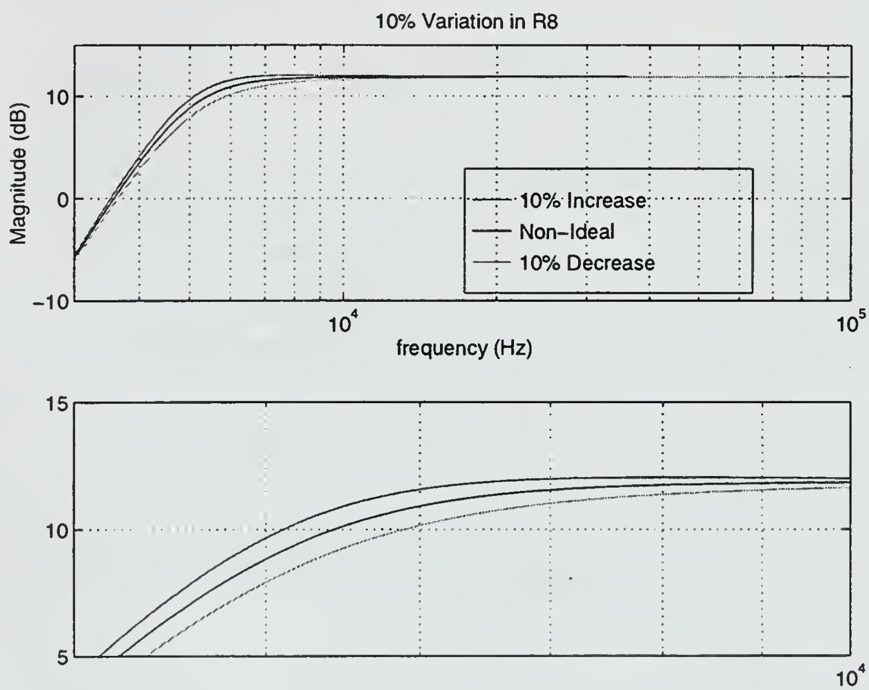



Figure 2.10: a) 10% Variation in R8 b) Magnified 10% Variation in R8

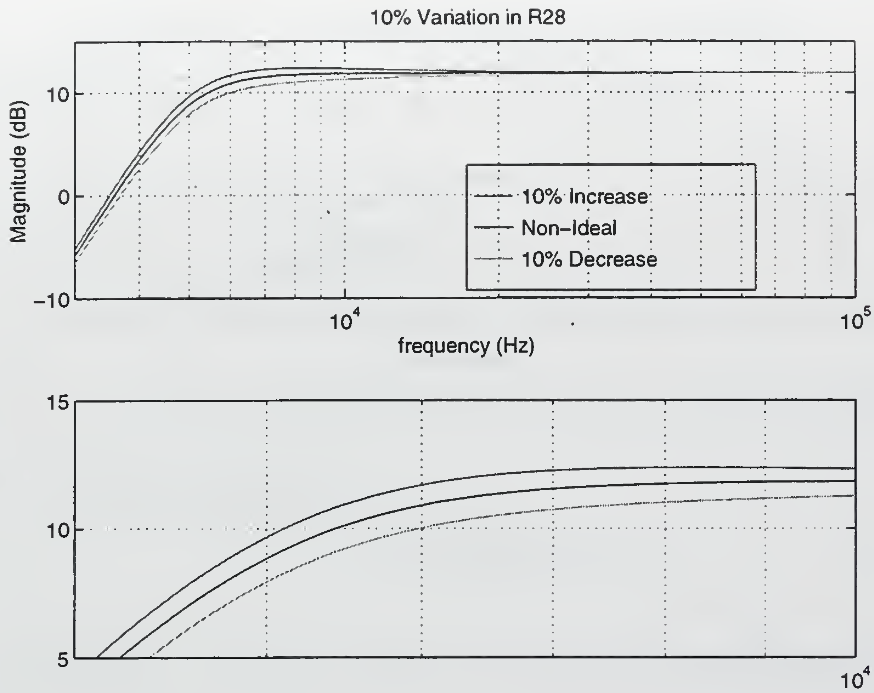



Figure 2.11: a) 10% Variation in R28 b) Magnified 10% Variation in R28

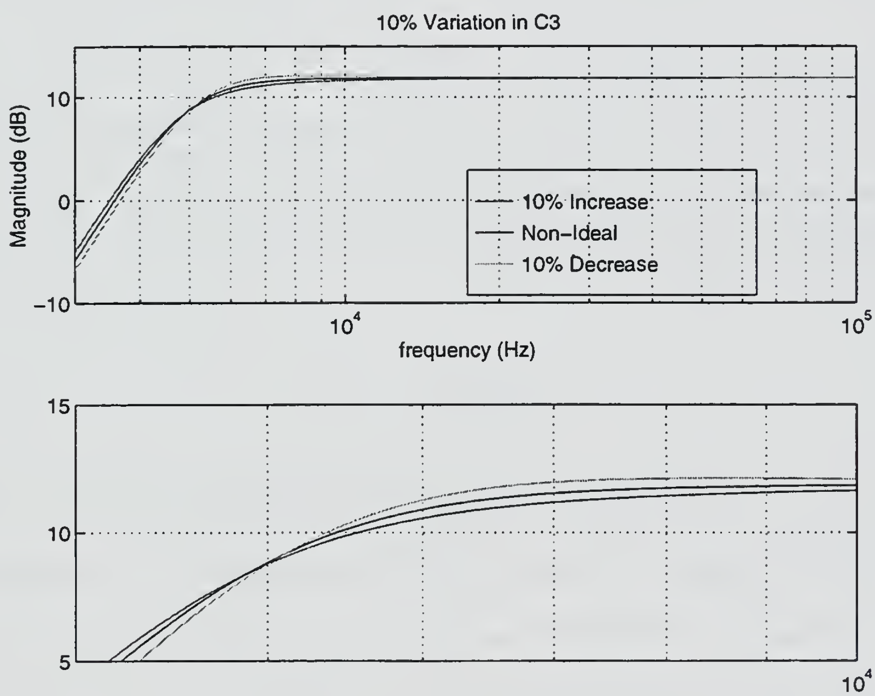



Figure 2.12: a) 10% Variation in C3 b) Magnified 10% Variation in C3

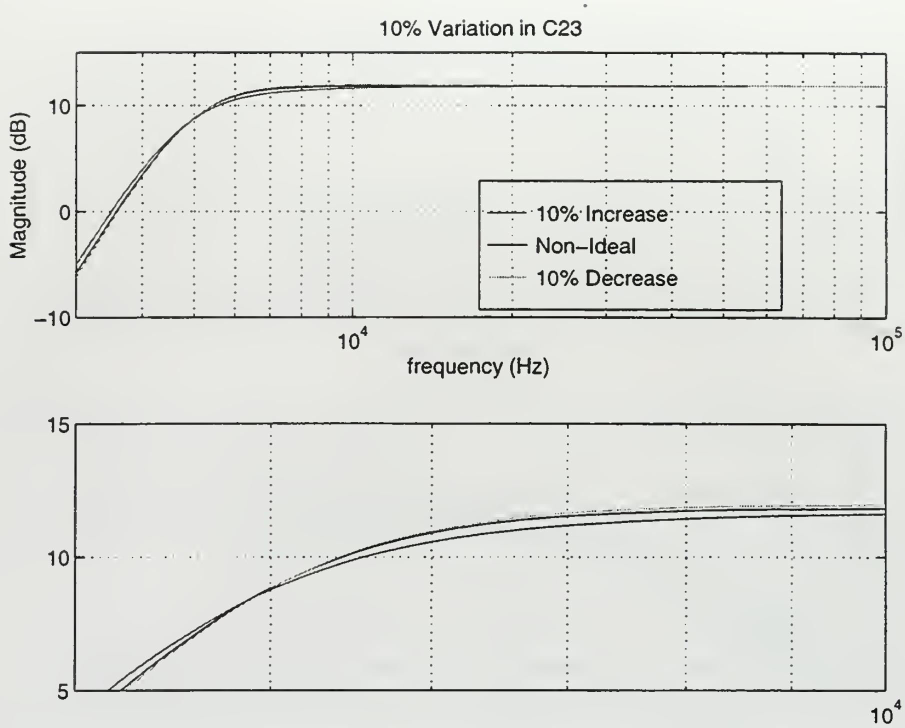



**Figure 2.13: a) 10% Variation in C23 b) Magnified 10% Variation in C23**

This chapter has set forth the evidence required to show that the GIC filter is a very attractive candidate for use with a non-ideal OP AMP and with components that may vary. The next chapter introduces the characteristics and operation of the switched capacitor implementation of the programmable GIC filter.

# III. SWITCHED CAPACITOR NETWORKS

## A. INTRODUCTION TO SWITCHED CAPACITORS

In semiconductor fabrication, it is very difficult to control the exact thickness, length, and width of the materials used in fabricating resistors. As a result, there are often large variations in the values of resistance implemented in VLSI designs. A resistor is relatively simple to create, but its value can vary up to 50%. The resistance of a uniform slab of conducting material may be expressed as

$$R = \left(\frac{\rho}{t}\right)\left(\frac{l}{w}\right) ohms \qquad \text{(Eq. 3.1)}$$

where $\rho$ = resistivity, t = thickness, l = conductor length, and w = conductor width. One method used, which provides good results, is laser trimming, but it is very expensive and still not exact. The switched capacitor technique seeks to replace the resistor in the circuit in order to provide a more accurate design. In today's VLSI designs, CMOS capacitors can be constructed within a tolerance of 0.1%. In order to tie together this discussion on component variations, the following example is presented. The filter center frequency for a given filter is set by the following RC product:

$$\omega_o = \frac{1}{RC} \qquad \text{(Eq. 3.2)}$$

Certainly if R varies by as much as 50%, then $\omega_o$ will also vary by as much as 50%. For precision designs one needs accurate values for all components. A designer will also require a predictable integrated circuit (IC) fabrication process [6]. The first step toward achieving very accurate parameter values is to realize $\omega_0$ using a ratio of capacitors. In the following, it will be shown that a switched capacitor, $C_R$, can represent an equivalent resistor value, R, such that

$$R = \left( \frac{1}{f_c C_R} \right) \qquad \text{(Eq. 3.3)}$$

where $f_c$ is the switching frequency. Therefore,

$$\omega_o = \frac{1}{T/_{C_R} C} = \frac{C_R}{C} f_c . \qquad \text{(Eq. 3.4)}$$

Thus, if we can implement a resistor with a switched capacitance then the large variation in center frequency can be eliminated.

Switched capacitor circuits operate on the principle that capacitors store a charge Q with a potential difference V. With a slight bias in one direction to achieve a net transfer of charge, one can achieve electric current flow. Therefore, if a capacitor $C_R$ is connected to a node with voltage $V_a$, it stores $Q_a = C_R V_a$. When connecting it to a subsequent node with voltage $V_b$, the capacitor will recharge to $Q_b = C_R V_b$. The charge transferred from $V_a$ to $V_b$ is

$$\Delta Q = Q_a - Q_b = C_R (V_a - V_b).$$

Figure 3.1 illustrates the switched capacitor network, with the switch being clocked on and off

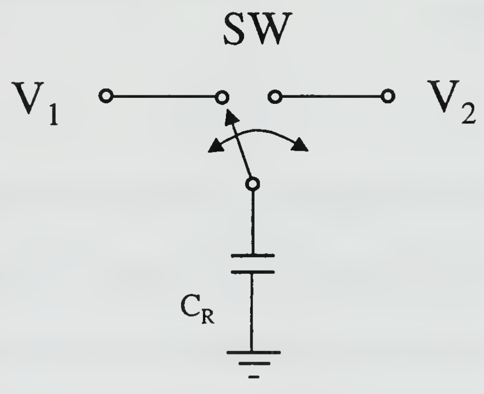



**Figure 3.1: Switch Capacitor Network**

at a rate $f_c = 1/T$. The clock frequency has to be much greater than the highest frequency component $(f_c >> f)$ of the input signal. As a consequence, the voltage signals will not change significantly over a switching period. Therefore, the average rate of transfer of charge $Q$ over the period T is considered current flow and may be expressed by

$$I \cong \frac{\Delta Q}{T} = \Delta Q f_c = f_c C_R (V_1 - V_2) \qquad \text{(Eq. 3.5)}$$

Dividing the potential difference by I, we obtain the expression for resistance

$$R \cong \frac{V_1 - V_2}{I} = \frac{1}{f_c C_R} \qquad \text{(Eq. 3.6)}$$

Actual implementation of the previous switching circuit is shown in Figure 3.2, where two Metal Oxide Semiconductor (MOS) switches are used to accomplish the switching task. This circuit requires two non-overlapping clock signals, $\Phi_1$ and $\Phi_2$, as depicted in Figure 3.3. The MOS transistors are switched on ('1' for closed) and off ('0' for open). In Figure 3.2, when t = nT, switch $S_1$ is closed momentarily to instantaneously charge the storage capacitor $C_R$ to

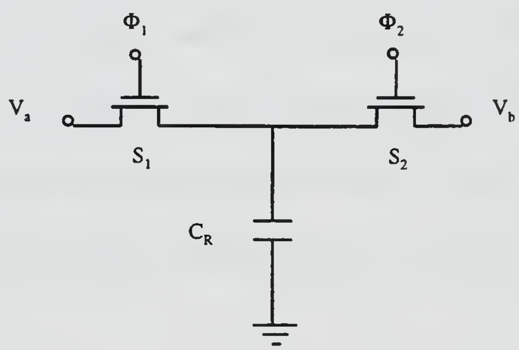



**Figure 3.2: Switched Capacitor with npn Transistors**

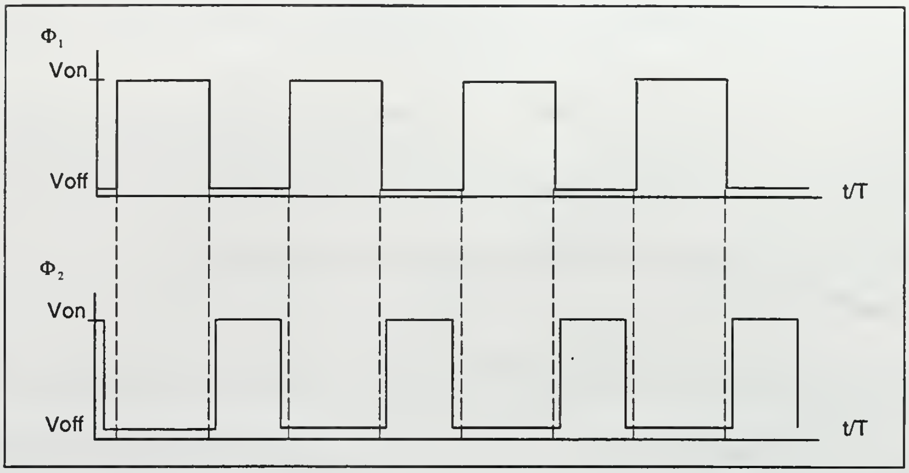



**Figure 3.3: Non-Overlapping Clock Output**

the value $V_a(nT)$. The capacitor then transfers all of the charge to node $V_b$ $\tau$ seconds later when switch $S_2$ is closed. In order for this to work properly, the non-overlapping two-phase clock of Figure 3.3 is required to prevent a direct short circuit that may occur if both switches are closed simultaneously [1].

## B. THE TWO-PHASE NON-OVERLAPPING CLOCK DESIGN

The two-phase clock is one of the most important parts of the Complementary Metal Oxide Semiconductor (CMOS) switched capacitor GIC filter design. MOS and CMOS devices will be discussed in detail in Chapter VI. The clock has to be non-overlapping and must have a sufficiently long duty cycle to allow proper charge transfer. Figure 3.4 shows the two-phase

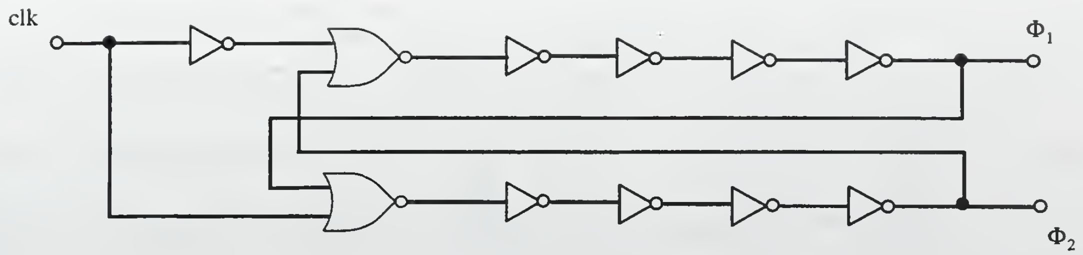



**Figure 3.4: Two-Phase Non-Overlapping Clock Circuit**

non-overlapping clock circuit. This design is based on a cross-coupled RS flip-flop. The external *clk* input is fed into an inverter and a NOR gate, producing opposite signals through the flip-flop. [7]

During initial Spice simulations the speed of each inverter pair was adjusted to ensure non-overlapping clock outputs. The speed of the inverters was adjusted by the size of NMOS or PMOS devices used. The Spice simulation schematic is shown in Figure 3.5.

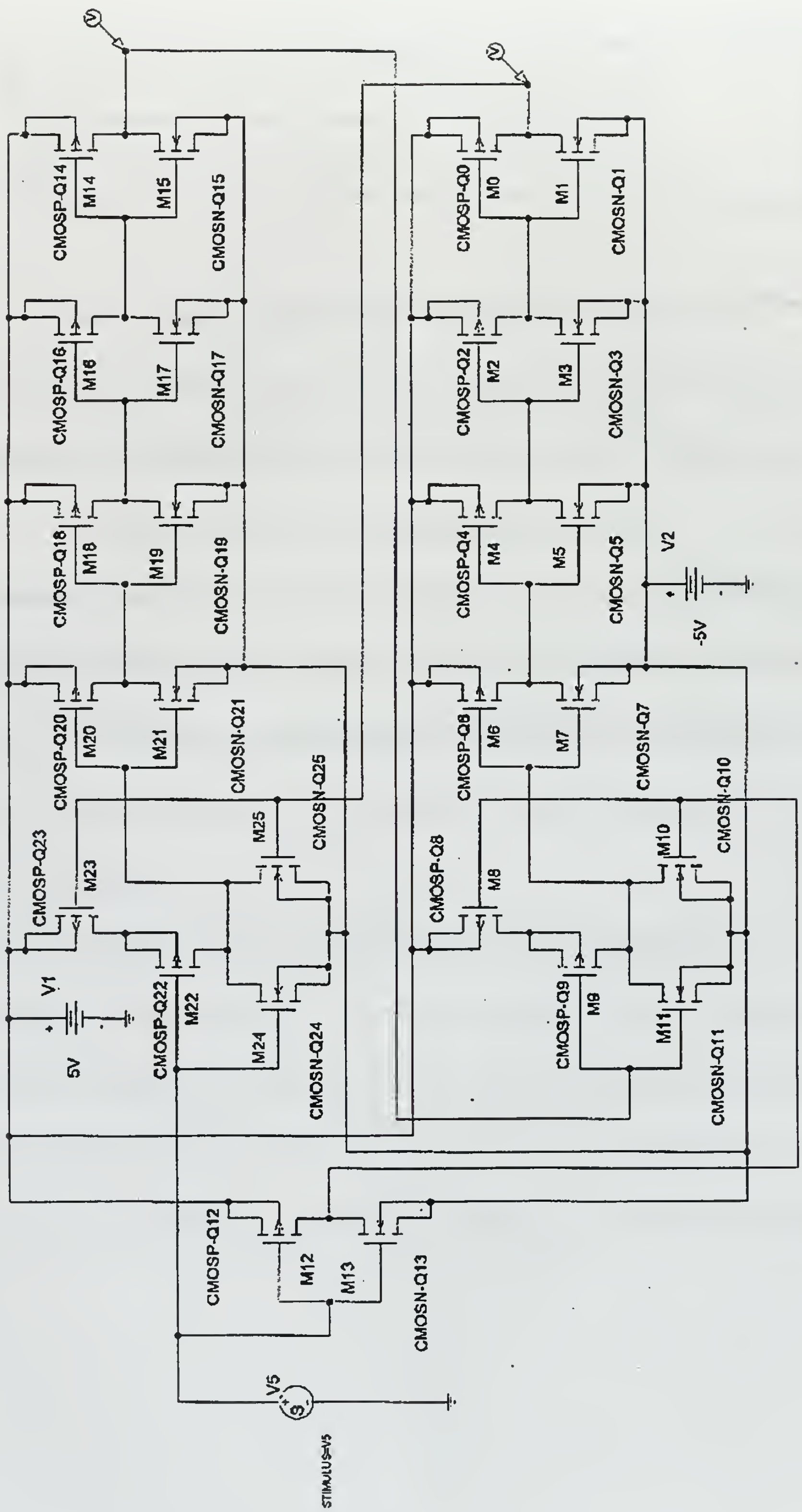



Figure 3.5: Spice Two-Phase Non-Overlapping Clock Schematic

Simulation of the two-phase clock was initiated with an input clock pulse of +5 volts at a frequency of 1 MHz. This clock enabled the overall circuit to provide two separate clock signals. The two signals were even and odd phases, non-overlapping at 1 MHz and are shown in Figure 3.6. Magnification of Figures 3.6 is provided in Figures 3.7 and 3.8. [8]

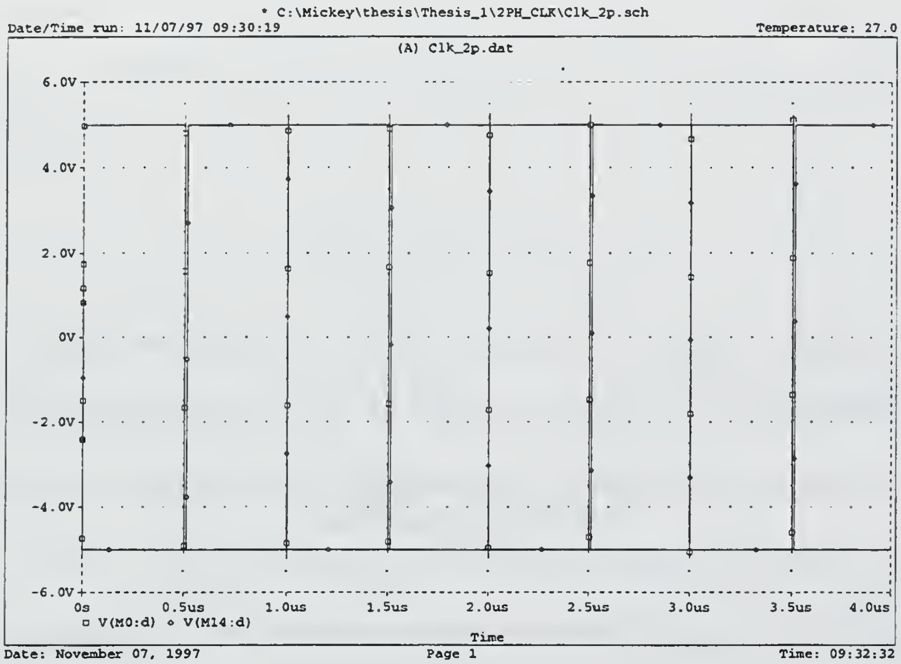



**Figure 3.6: Two-Phase Non-Overlapping Clock Spice Simulation Output**

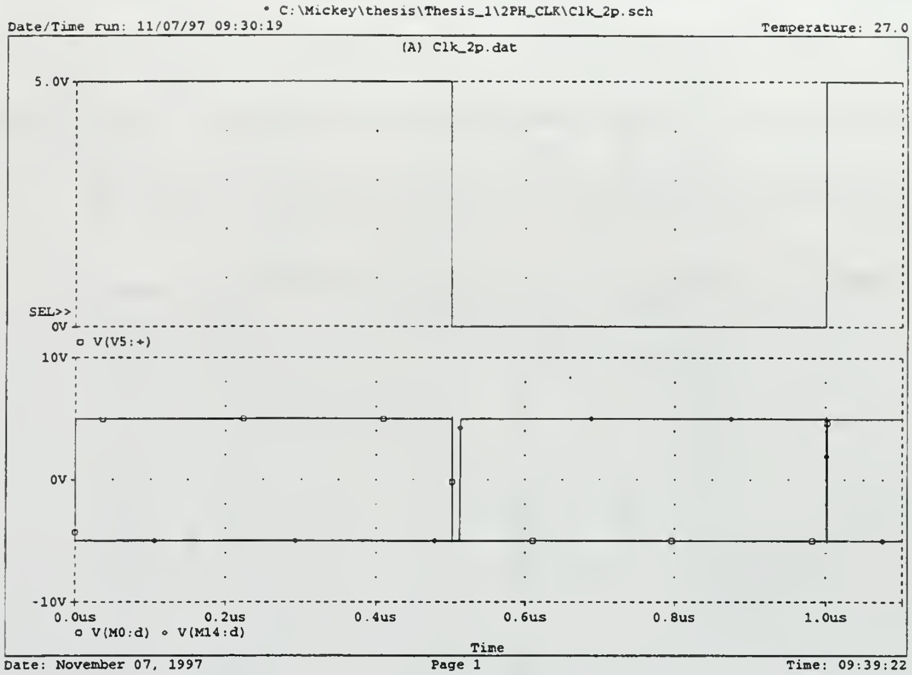



**Figure 3.7: a). Input Clock Signal b). The Magnified Spice Output of the Two-Phase Non-Overlapping Clock**

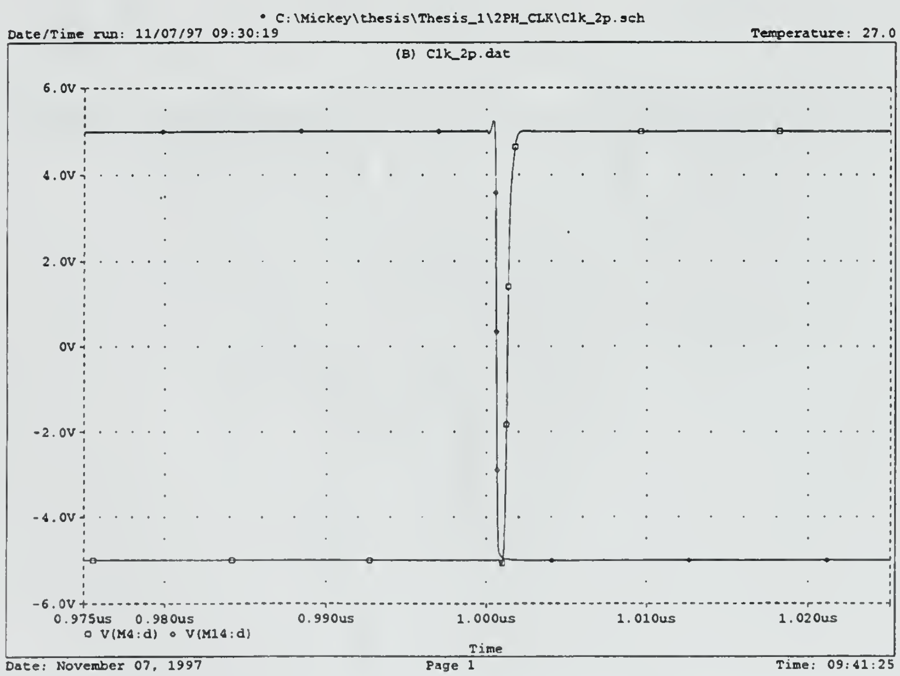



**Figure 3.8: The Magnified Spice Output of the Two-Phase Non-Overlapping Clock**

## C. CONTINUOUS/DISCRETE

Since switched capacitor networks use sampled-data techniques similar to digital filter applications, the z-transform is the appropriate analysis tool. When applying the z-domain analysis to a continuous system, the transformation must be such that it maintains the s-domain equivalency. If we consider a model of a continuous-time filter with a transfer function $H_a(s_a)$, the system response is then determined by the following system of first-order differential equations

$$\frac{dx_i(t)}{dt} = g_i(t), \quad i = 1, 2, ..., N. \qquad \text{(Eq. 3.7)}$$

where $x_i$ are the state variables of the filter. The $g_i(t)$ terms are the linear functions of the state variables $x_i(t)$ and the input signal. Using the Laplace transformation, we obtain from (Eq. 3.7)

$$S_a X_i(s_a) = G_i(s_a), \quad i = 1, 2, ..., N. \qquad \text{(Eq. 3.8)}$$

where $x_i(t) = 0$ for $t \le 0$ and an analog model is indicated by using the subscript (a) [9].

Equations of a sampled-data system, which can realize the same continuous-time filter previously mentioned, are related to each other by a first-order difference equation. The difference equation can be found by integrating (Eq. 3.8) and using (n-1)T and nT as the limits of integration. The integration yields

$$\int_{(n-1)T}^{nT} \frac{dx_i(t)}{dt} dt = x_i(nT) - x_i(nT - T) = \int_{(n-1)T}^{nT} g_i(t) dt, \; i = 1, 2, ..., N. \qquad \text{(Eq. 3.9)}$$

The approximation of the integral may be accomplished using either Euler or trapezoidal formulas. In general, the trapezoidal formulas are more accurate. This method can be used if the area under the curve for $(n-1)T \le t < nT$ is approximately that of a trapezoid. From this approximation, (Eq. 3.9) becomes

$$\int_{(n-1)T}^{nT} g_i(t)dt \cong \frac{T}{2}\left[g_i(nT-T)+g_i(nT)\right]. \qquad \text{(Eq. 3.10)}$$

Therefore, from (Eq. 3.9) and (Eq. 3.10), the following equation holds:

$$x_i(nT)-x_i(nT-T) \cong \frac{T}{2}\left[g_i(nT-T)+g_i(nT)\right]. \qquad \text{(Eq. 3.11)}$$

A graphical representation of the trapezoidal method is illustrated in Figure 3.8.

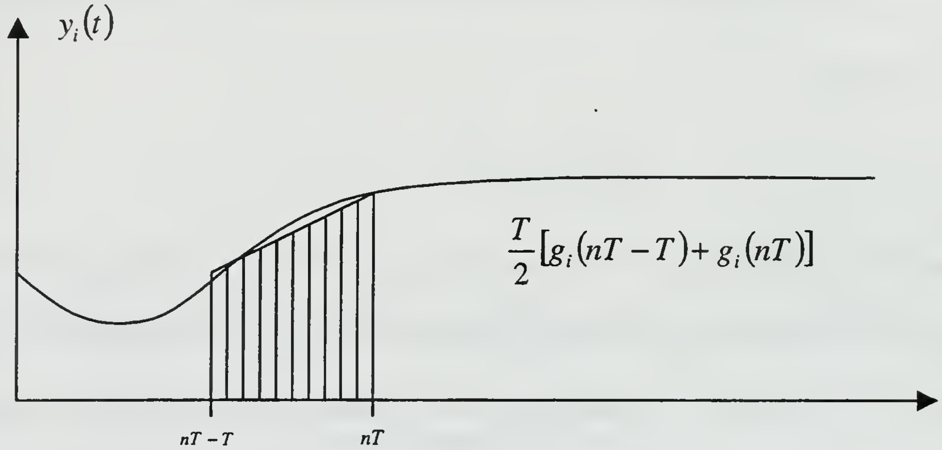



**Figure 3.9: Trapezoidal Integration Technique**

Upon application of the z-transformation, (Eq. 3.11) becomes

$$\frac{2}{T}\frac{z-1}{z+1}X_i(z)=G_i(z) \qquad \text{(Eq. 3.12)}$$

By using the trapezoidal integration technique (the Bilinear Transform), designers can show a relationship between the variable s in the s-domain and the variable z in the z-domain. In particular,

$$s_a = \frac{2}{T}\frac{z-1}{z+1} \qquad \text{(Eq. 3.13)}$$

There are two requirements for the transformation method. The first requirement is to map stable s-domain functions into stable z-domain functions. The second requires mapping the $j\omega - axis$ in the s-plane to the unit circle in the z-domain. The first of these requirements

ensures the network stability. The second of these requirements will ensure the preservation of gain response. A designer can test the ability of the transformation techniques to meet the requirements by setting $s = -\sigma + j\omega$ and analyzing z for different stable values of s.

With $s = j\omega_a$,

$$|z| = \left| \frac{1 + j\omega_a \, T/2}{1 - j\omega_a \, T/2} \right| = 1 \qquad \text{(Eq. 3.14)}$$

Stable s-plane poles are mapped into stable z-domain poles by using the above bilinear transformation method. This same method also maps the s-plane $j\omega - axis$ to the unit circle in the z-plane. Figure 3.10 shows the results of the bilinear transformation. This technique is considered to be satisfactory for performing the mapping function. The bilinear transformation technique is a preferred choice in switched capacitor network applications [9].

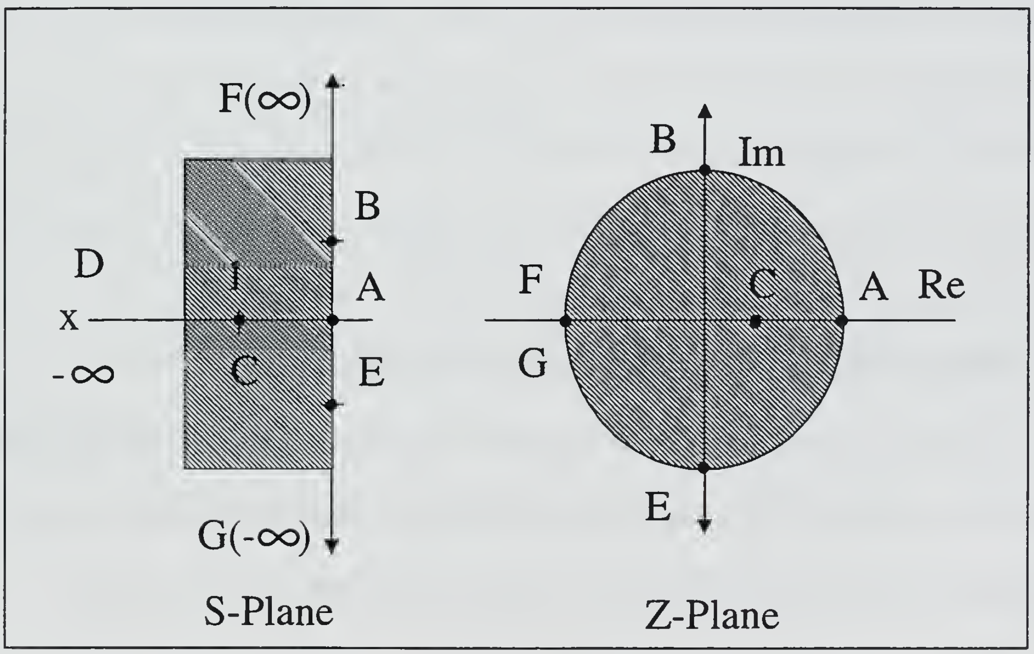



**Figure 3.10: Bilinear Transformation Results**

## D. BILINEAR TRANSFORMATION SIDE EFFECTS

The transformation from the s-domain to the z-domain has some drawbacks. Even though the mapping of s-plane poles to z-plane poles meet the aforementioned requirements, some imperfections or side effects must be discussed. By solving (Eq. 3.15) for s,

$$s_a = \frac{2}{T}\frac{z-1}{z+1}, \qquad \text{(Eq. 3.15)}$$

substituting $e^{j\omega T}$ for z and dividing both the numerator and denominator by $2e^{j\omega T/2}$, we obtain

$$\frac{\omega_a T}{2} = \tan\frac{\omega T}{2} \qquad \text{(Eq. 3.16)}$$

Further, solving (Eq. 3.16) for $\omega$, we get

$$\omega = \frac{2}{T}\tan^{-1}\left[\frac{\omega_a T}{2}\right] \qquad \text{(Eq. 3.17)}$$

The difference between a given frequency in either network, analog or switched capacitor, is described in (Eq. 3.17). The major drawback, commonly called warping, comes from the transformation of a straight line from the s-domain to the unit circle in the z-domain. The designer needs to minimize potential warping by maintaining a clock frequency at least ten times greater than that of the analog signal frequency [10].

## E. THE BILINEAR SWITCHED CAPACITOR RESISTOR

This section covers the development of the floating bilinear switched capacitor resistor. This type of resistor is used in the implementation of the GIC filter. The switched capacitor network depicted in Figure 3.11 will be studied using nodal analysis. The 'e' in the Figure

denotes 'even phase' while 'o' denotes 'odd phase'. As illustrated in Figure 3.11, two separate nodal equations can be generated: one for when the 'o' switches are closed and one for when

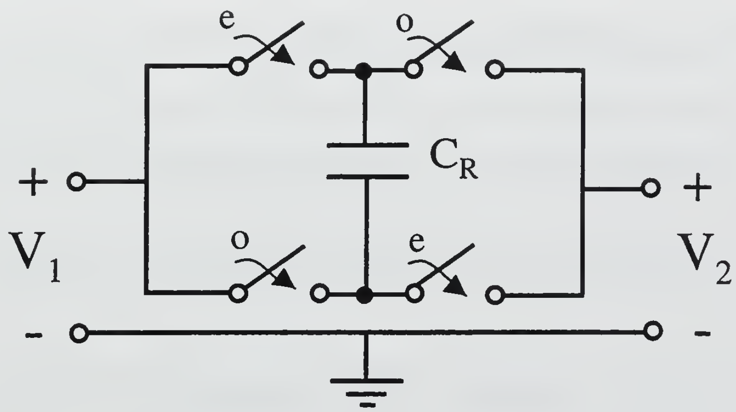



**Figure 3.11: Floating Bilinear Resistor**

the 'e' switches are closed. The clock period shown in Figure 3.7a is denoted by $\tau$, where the period $T = \tau/2$. The sampling rate is kT where $\Delta q(kT)$ represents the instantaneous charge at either node for the even and odd sampling periods.

For even kT times:

$$\Delta q_1^e(kT) = Cv_1^e(kT) - Cv_1^o[(k-1)T] - Cv_2^e(kT) - Cv_2^o[(k-1)T] \qquad \text{(Eq. 3.18)}$$

$$\Delta q_1^e(kT) = Cv_2^e(kT) - Cv_2^o[(k-1)T] - Cv_1^e(kT) - Cv_1^o[(k-1)T] \qquad \text{(Eq.3.19)}$$

For odd kT times:

$$\Delta q_1^o(kT) = Cv_1^o(kT) - Cv_1^e[(k-1)T] - Cv_2^o(kT) - Cv_2^e[(k-1)T] \qquad \text{(Eq. 3.20)}$$

$$\Delta q_1^o(kT) = Cv_2^o(kT) - Cv_2^e[(k-1)T] - Cv_1^o(kT) - Cv_1^e[(k-1)T] \qquad \text{(Eq. 3.21)}$$

From the z-transform, where $Z[u(kT)] = U(z)$ and $Z[u[(k-1)T]] = z^{-1/2}U(z)$, the nodal charge equations can be found. With Q=CV, the charge equations for the floating bilinear switched capacitor resistor of Figure 3.11 are shown to be as follows:

$$\Delta Q_1^e(z) = CV_1^e(z) + Cz^{-1/2}V_1^o(z) - \left(CV_2^e(z) + Cz^{-1/2}V_2^o(z)\right) \quad \text{(Eq. 3.22)}$$

$$\Delta Q_1^o(z) = CV_1^o(z) + Cz^{-1/2}V_1^e(z) - \left(CV_2^o(z) + Cz^{-1/2}V_2^e(z)\right) \quad \text{(Eq. 3.23)}$$

$$\Delta Q_2^e(z) = CV_2^e(z) + Cz^{-1/2}V_2^o(z) - \left(CV_1^e(z) + Cz^{-1/2}V_1^o(z)\right) \quad \text{(Eq. 3.24)}$$

$$\Delta Q_2^o(z) = CV_2^o(z) + Cz^{-1/2}V_2^e(z) - \left(CV_1^o(z) + Cz^{-1/2}V_1^e(z)\right) \quad \text{(Eq. 3.25)}$$

The above equations can be simplified by adding the two equations governing each node.

$$\Delta Q_1(z) = C\left(1 + z^{-1/2}\right)V_1(z) - C\left(1 + z^{-1/2}\right)V_2(z) \quad \text{(Eq. 3.26)}$$

$$\Delta Q_2(z) = C\left(1 + z^{-1/2}\right)V_2(z) - C\left(1 + z^{-1/2}\right)V_1(z) \quad \text{(Eq. 3.27)}$$

Reducing (Eq. 3.26) and (Eq. 3.27), we get

$$\Delta Q_1(z) = YR(V_1(z)) - YR(V_2(z)), \quad \text{(Eq. 3.28)}$$

$$\Delta Q_2(z) = YR(V_2(z)) - YR(V_1(z)). \quad \text{(Eq. 3.29)}$$

Combining the above equations, we obtain

$$\Delta Q_1 - \Delta Q_2 = [(YR(V_1(z)) - YR(V_2(z))) - (YR(V_2(z)) - YR(V_1(z)))] \quad \text{(Eq. 3.30)}$$

$$\Delta Q = YR\Delta V_1 - YR\Delta V_2 \quad \text{(Eq. 3.31)}$$

Given that $z = e^{sT}$ for a half clock cycle, (Eq. 3.32) is obtained:

$$YR = C\left(1 + z^{-1/2}\right) \quad \text{(Eq. 3.32)}$$

On the other hand, given $\hat{z} = e^{s\tau/2}$ for a full clock cycle:

$$YR = C\left(1 + z^{-1}\right) \qquad \text{(Eq. 3.33)}$$

Before finishing the nodal analysis on the floating bilinear resistor, we must first find the element transformations for each component. The following element transformations can be found in Ref. [10, 11]. It can be shown that due to the sampling the switch capacitor networks are time dependent. Studying the current and voltage relationship across a resistor, capacitor and inductor the following bilinear transformation equivalences can be easily derived.

| | Capacitor | Resistor | Inductor |
|---|---|---|---|
| Laplace Domain | C | $G/s$ | $1/Ls^2$ |
| Bilinear Transformation | $C\left(1+z^{-1}\right)$ | $\dfrac{G\tau\left(1+z^{-1}\right)}{2}$ | $\dfrac{\tau^2\left(1+z^{-1}\right)^2}{4L\left(1-z^{-1}\right)}$ |

**Table 3.1: Z-domain Scaled Admittances (from Ref. [11])**

Now using the bilinear resistor equation from Table 3.1, $\left(\dfrac{G\tau\left(1+z^{-1}\right)}{2}\right)$, and setting it equal to the admittance of a resistor [11], the following simplification can occur. Equation 3.35 shows that a desired admittance can be achieved with appropriate clock frequencies.

For half a clock cycle:

$$C\left(1+z^{-1}\right) = \frac{G\tau\left(1+z^{-1}\right)}{2} \qquad \text{(Eq. 3.34)}$$

where

$$G = \frac{2C}{\tau} \qquad \text{(Eq. 3.35)}$$

and for a full clock cycle:

$$G = \frac{4C}{\tau}. \qquad \text{(Eq. 3.36)}$$

The GIC or switched capacitor filter network can be realized best by reducing the warping effects and then choosing a capacitor to fit your circuit.

## F. SPICE SIMULATION OF THE BILINEAR SWITCHED CAPACITOR RESISTOR

Two transistors biased on and off with the non-overlapping clock signals $\Phi_1$ and $\Phi_2$ will realize the bilinear resistance for a GIC filter. The input signals *in_even* and *in_odd* are $\phi_1$

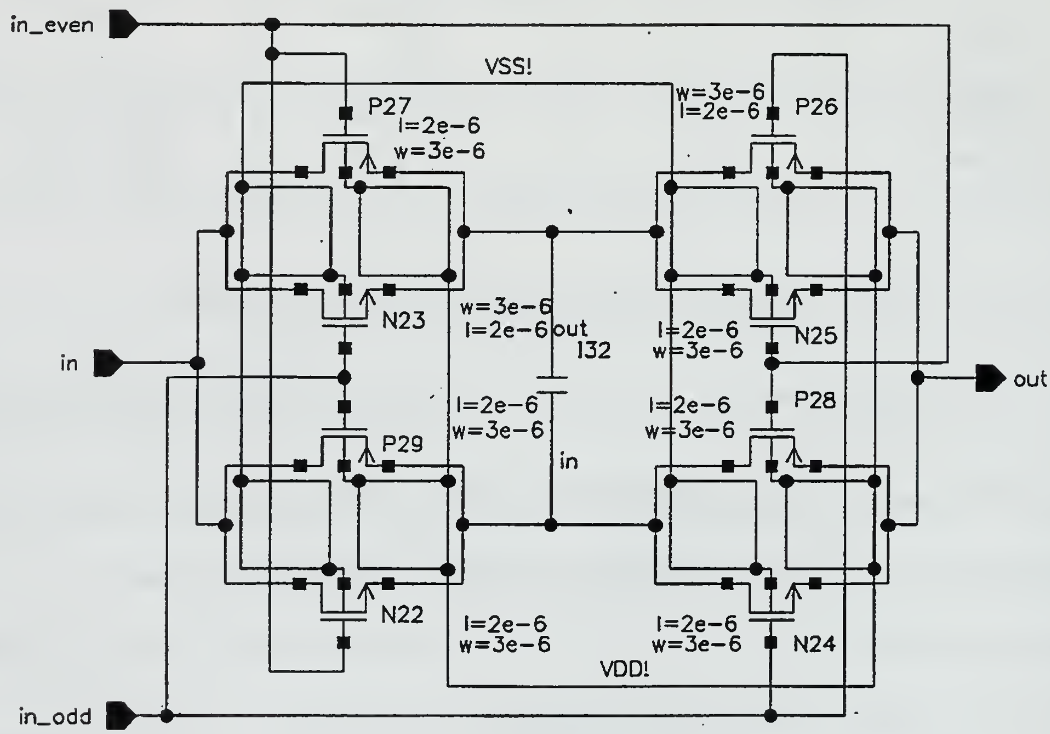



**Figure 3.12: Bilinear Switched Capacitor Resistor**

and $\phi_2$ respectively. The Spice simulation was initiated with the two phase non-overlapping clock operating at 100 kHz. A 1nf switched capacitor is used to realize the resistor. The value of R implemented is

$$R = \left(\frac{\tau}{4C}\right) = \frac{1/f}{4C} = \frac{1/100kHz}{4(1nf)} = 2500\Omega \,. \qquad \text{(Eq. 3.37)}$$

For the given circuit considered, the resistance network yields a voltage divider that will theoretically scale the input by one half. With an input sine wave of 100mV, it can be concluded that a 50mV output is expected. The Spice simulation schematic is shown in Figure 3.13, and the simulation output results are shown in Figure 3.14. The output is indeed one half the input, thus validating (Eq. 3.37). An additional simulation was completed with the following changes: the clock frequency is increased to 200 kHz and the switched capacitance is decreased to 0.5nf. Again the output shows a fifty-percent reduction in the input signal at the (see Figure 3.15) output. The Spice netlist and output files for these simulations are listed in Appendix B. [8]

The next Chapter introduces the operational amplifier and why we chose the Silvernagle operational amplifier for this research.

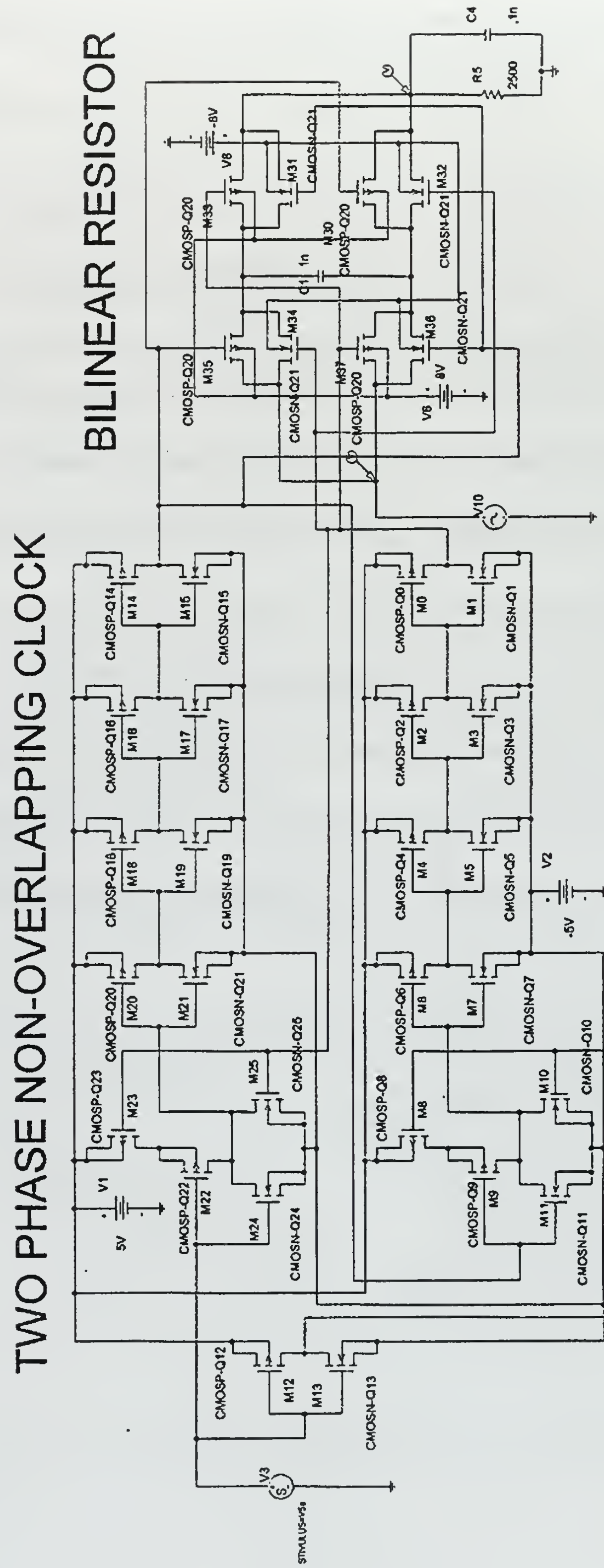



Figure 3.13: Spice Simulation of the Bilinear Switched Capacitor Resistor

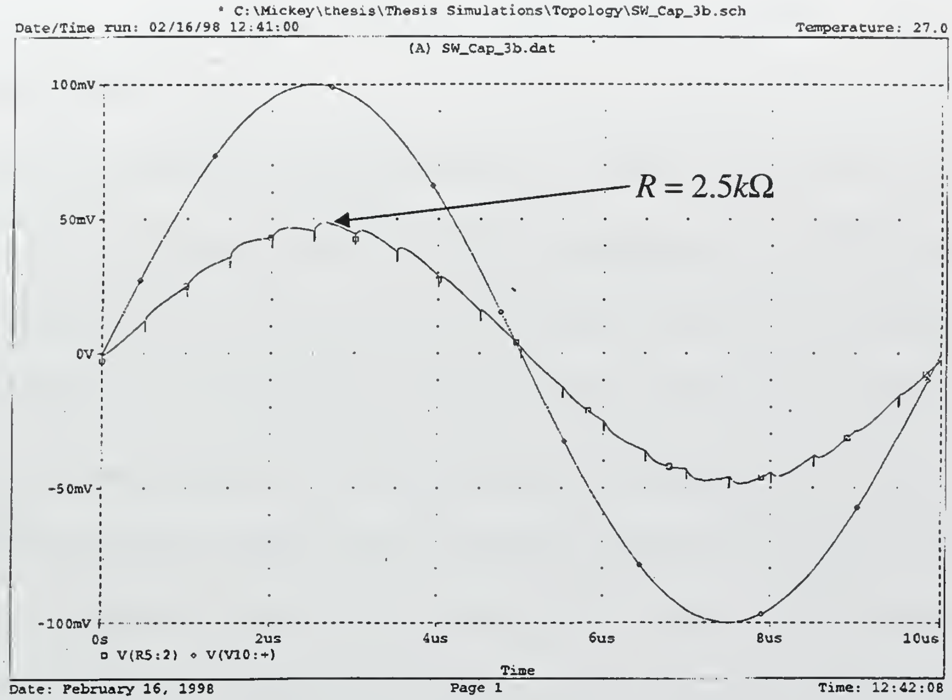



**Figure 3.14: Spice Simulation Output of the Bilinear Switched Capacitor Resistor with $f_c$ =1 00 kHz and $C_R$ = 1 nf**

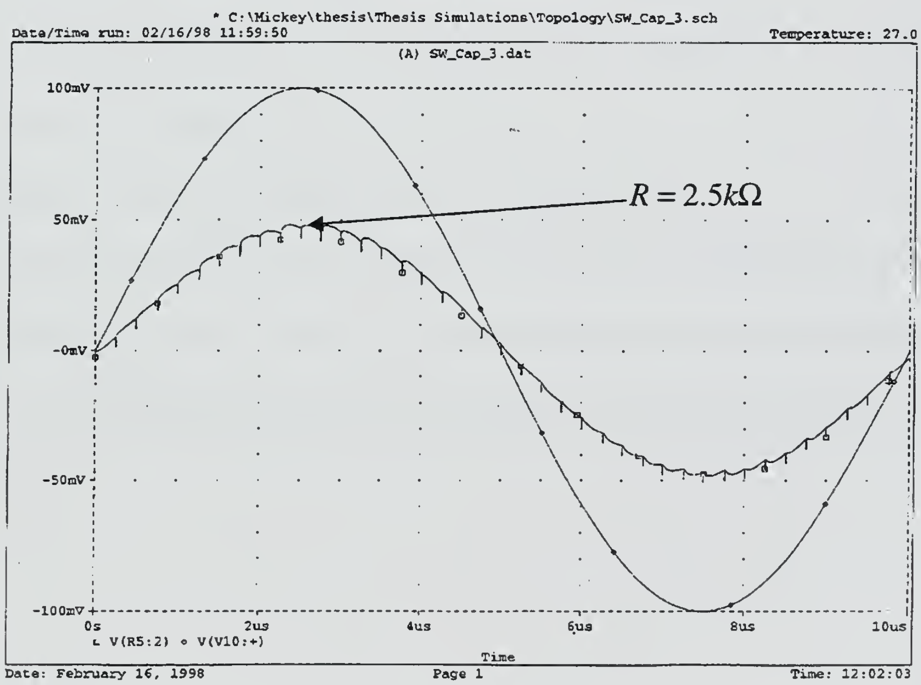



**Figure 3.15: Spice Simulation Output of the Bilinear Switched Capacitor Resistor with $f_c$ = 200 kHz and $C_R$ = 0.5 nf**

# IV. THE OPERATIONAL AMPLIFIER

## A. INTRODUCTION

In 1965, Fairchild Semiconductor introduced the $\mu A709$, the first widely used monolithic OP AMP. Although highly successful, this first generation OP AMP had many disadvantages. This led to the development of a more improved OP AMP known as the $\mu A741$ in 1970. Because it is inexpensive and easy to use, the $\mu A741$ has been widely used in numerous applications. Many other 741-derived designs have appeared from various manufacturers. Inevitably, general purpose OP AMPs were redesigned to optimize or add certain features. Special function ICs that contain more than a single OP AMP were developed to perform complex functions such as a flash AD converter. One should expect to see a continued rapid development of more and more highly complex integrated circuits on a single microchip. These chips will continue to combine OP AMPs with digital circuitry. In fact, with improved Very Large-Scale Integrated (VLSI) technology, it is inevitable that entire systems will be fabricated on a single chip. [5]

## B. EXAMINING THE OPERATIONAL AMPLIFIER

Real OP AMPs depart from the ideal in two important ways: limitations on operating frequency (bandwidth) and on output voltage swing (usually closely related to the voltage supplied). The following nine subsections define terms associated with OP AMP characterization.

### 1. Input Bias Current

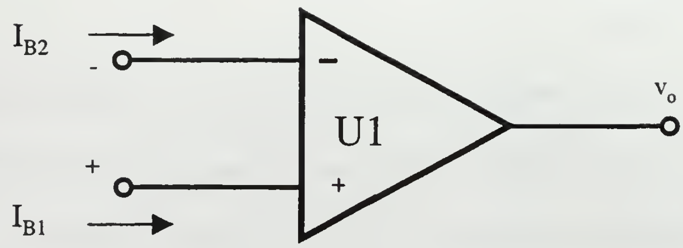



**Figure 4.1: Circuit Symbol For The OP AMP**

Ideally the input bias currents $(I_{B1})$ and $(I_{B2})$ should be zero (referring to Figure 4.1), but in real-world applications the OP AMP requires small dc currents for operation. Typical values are 10 to 100 nA for bipolar input devices, and less than 0.001 pA for MOSFET input devices. The average value $I_B$ is defined as the input bias current.

$$I_B = \frac{I_{B1} + I_{B2}}{2} \qquad \text{(Eq. 4.1)}$$

The difference between the two input bias currents is called input offset current and is defined as

$$I_{os} = |I_{B1} - I_{B2}| \qquad \text{(Eq. 4.2)}$$

For example, for the 741 OP AMP, the input bias current is on the order of 40 nA and the input offset current is on the order of 5 nA.

### 2. Input Offset Voltage

Given that there is no differential voltage between the inverting and non-inverting inputs of the OP AMP, ideally there would be no output voltage. However, OP AMPs generally require several mV of differential input to zero out the output. This nulling input signal is defined as input offset voltage, $v_{os}$. It ranges from 1 to 5 mV for bipolar input devices and 1 to 20 mV for FET devices.

### 3. Common Mode Rejection Ratio (CMRR)

A common-mode signal is a signal common to both inputs of the OP AMP simultaneously. This can be expressed by connecting both inputs together as shown in Figure 4.2 and supplying an input signal $v_{in}$. The CMRR is evaluated from

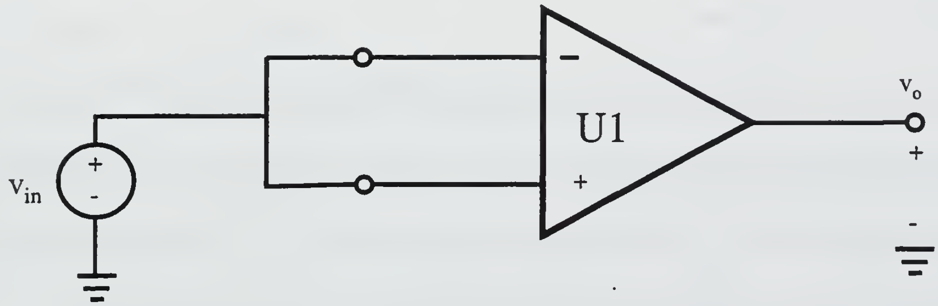



**Figure 4.2: CMRR Circuit**

$$CMRR = 20\log\frac{|A|}{|A_{cm}|} \qquad \text{(Eq. 4.3)}$$

where $A$ is the differential gain of the open-loop OP AMP and $A_{cm}$ is the ratio ${v_o}/{v_{in}}$. The CMRR is a measure of the ability of an operational amplifier to reject signals, such as noise, present simultaneously at both inputs.

### 4. Input Impedance

The ratio of input voltage to input current is called the input impedance. For an ideal amplifier, it should be infinite, but typically it ranges from 100 kΩ to 2 MΩ for the 741 OP AMP and essentially infinite for CMOS OP AMPs.

### 5. Output Impedance

Output impedance is the ratio of open-circuit output voltage to short circuit output current. For an ideal amplifier, it should be zero, but typically it ranges from 40 to 100 $\Omega$ for bipolar OP AMPs. For a real MOS OP AMP output impedance is usually resistive and on the order of 100 to 5,000$\Omega$.

### 6. Frequency Response

The frequency response characteristics of an OP AMP is a vital operating parameter. Because of stray parasitic capacitance, the open-loop transfer function of an OP AMP has additional poles. For the 741 OP AMP, these poles are typically at 2-3 MHz and 8 MHz. A 741 OP AMP rolls off at -20-dB/decade (typical for internally compensated) with a bandwidth of 1 MHz. This effect can be described in terms of the Unity Gain Bandwidth, which is defined as being the frequency at which the frequency response magnitude is equal to unity. Typical values for MOS OP AMPs are in the range of 1-10 MHz. Measuring the Unity Gain Bandwidth can be achieved by connecting the OP AMP in the voltage-follower configuration.

### 7. Slew Rate

Slew rate is the rate of change of the output voltage with respect to time $\left(\frac{dv_o}{dt}\right)$. In particular, the output is measured following the application of a large input signal (a prefect step input function). Typical values are on the order of a few $V/\mu s$. For MOS OP AMPS, slew rates of 1-20 $V/\mu s$ can be obtained.

### 8. Finite DC Gain

For practical OP AMPS, dc voltage gain is finite. Actual values for low frequency and small signals range from an absolute value of 100 to $10^6$.

$$Gain(dB) = 20\log\frac{V_o}{v_i} \qquad \text{(Eq. 4.4)}$$

### 9. Finite Linear Range

The linear relationship between the input and output voltages are only valid for a finite range. This range can be equal to a value just below the dc power supplied to the OP AMP shown in Figure 4.3. For example, the range for a $\mu A741$ is around 12 V for the positive

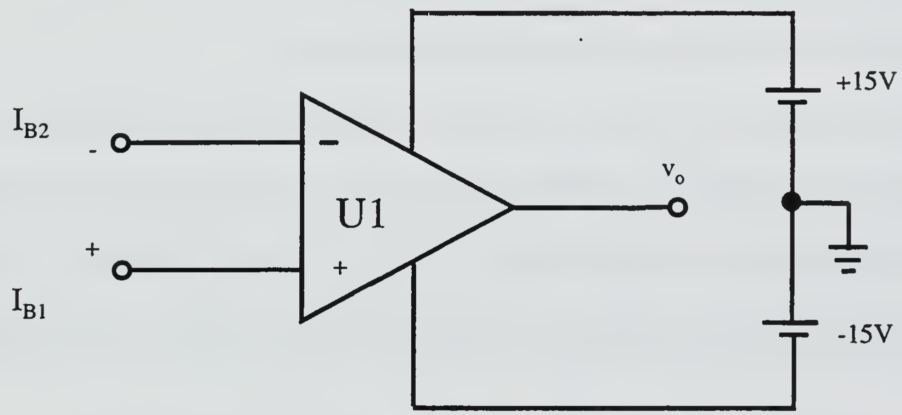



**Figure 4.3: OP AMP Connected To Dc Power Supply**

supply and -11 V for the negative supply. This value is not constant for all OP AMPs and each type of OP AMP has a different linear range. Finite linear range is the maximum output voltage without clipping.

## C. METAL OXIDE SEMICONDUCTOR (MOS) OPERATIONAL AMPLIFIER

MOS OP AMPs consist of a number of metal-oxide-semiconductor field effect transistors (MOSFET). Upon superimposing several layers of conducting, insulating and

transistor forming material together, semiconductor fabricators can realize electronic components such as OP AMPs. These OP AMPs have virtually no resistors or other components with the exception of the MOSFETs. This technology is increasing in popularity because MOSFET elements permit a much greater complexity and take up less chip space (chip real estate). This facilitates more complex circuitry, smaller gate sizes, and faster speeds in the same amount of area. The function of the MOSFET differs from that of a PNP transistor because Bipolar Junction Transistors (BJT) are current devices and MOSFETs are voltage-controlled devices. The MOSFET is turned on with an applied electric field created by the gate voltage. The MOS transistor is turned on and off by the gate controlling the passage of current between the source and the drain. This process will be discussed in-depth in Chapter VI.

## D. TESTING THE OPERATIONAL AMPLIFIER

Silvernagle initially developed the operational amplifier considered in this thesis. However, the layout in Cadence was completed without the aid of Silvernagle's OP AMP layout. The schematic of the OP AMP is shown in Figure 4.4, and the VLSI layout is shown in Appendix D. Research efforts regarding the Silvernagle OP AMP can be found in Ref.[12].

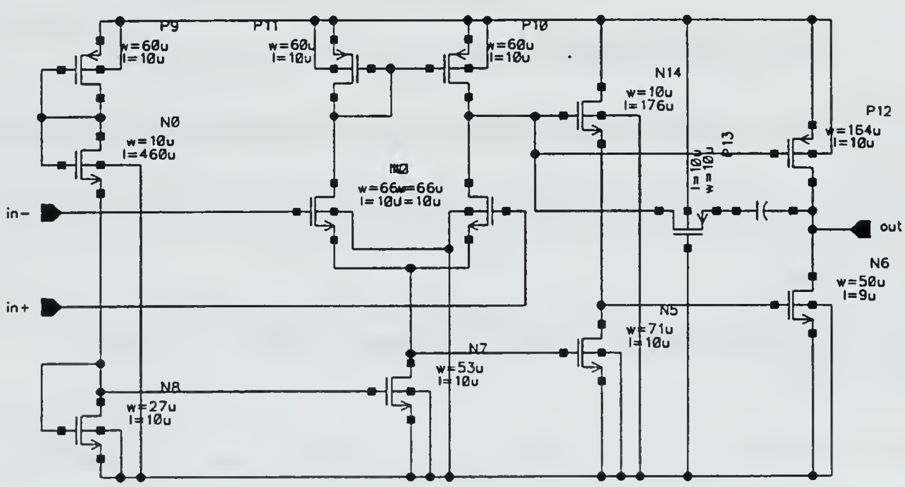



**Figure 4.4: Schematic View Of The Silvernagle Operational Amplifier**

An ideal OP AMP (Figure 4.5) may be modeled as a voltage–controlled voltage source with an infinite voltage gain. The input resistance is considered to be infinite and the output

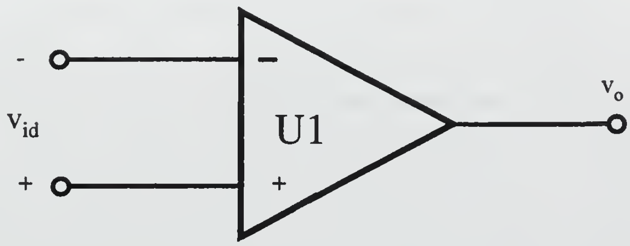



**Figure 4.5: Ideal OP AMP**

resistance is considered to be zero. Unfortunately, Spice does not allow infinite values, so the infinite gain voltage source can not be modeled as such. A designer must compromise and use a finite voltage gain around $10^6 \, {}^{V}\!/_{V}$. When these constraints are used on the OP AMP, it can no longer be called ideal, but rather pseudo-ideal [8].

The simulation schematic in Spice is shown in Figure 4.6. This circuit was investigated by applying a 0.1 mV input sine wave at 100 Hz. This input signal was supplied to the positive input terminal with the negative input terminal grounded. It is anticipated that the OP AMP

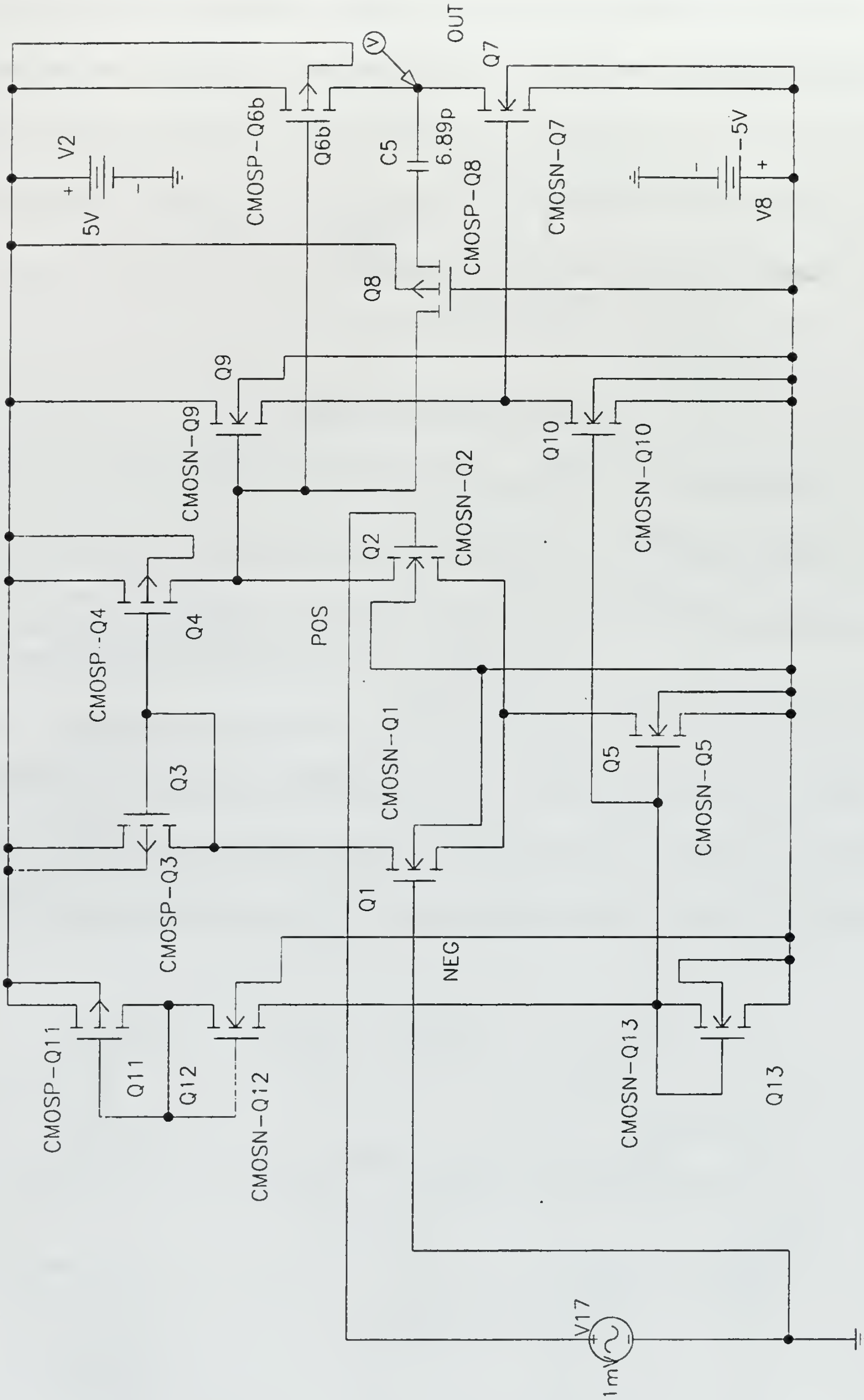



Figure 4.6: Silvernagle OP AMP Simulation In Spice

will amplify the input by a factor of at least 1000 times. Results of this investigation are documented in Figure 4.7.. Once it was determined the circuit was operating correctly it was then tested for slew rate and Gain-Band-Width Product (GBWP) [8].

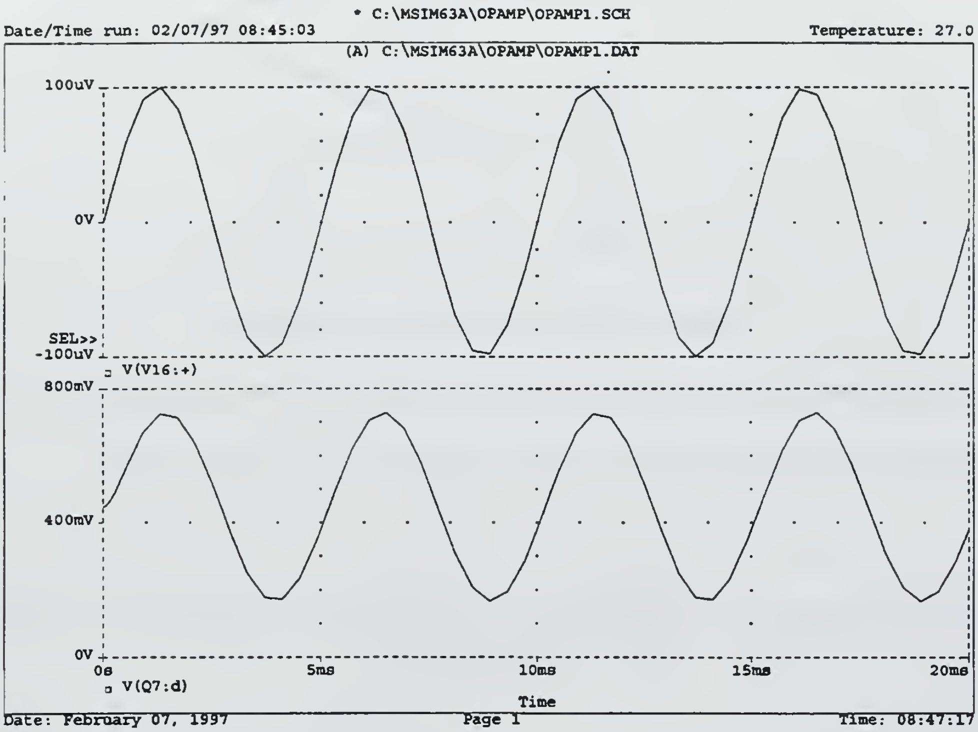



**Figure 4.7: Spice Output Signal From The Silvernagle OP AMP**

A cause of non-linear distortion is slew rate. A designer can find the slew-rate by applying a progressively larger step input into the OP AMP, with the OP AMP in a unity-gain follower configuration, as shown in Figure 4.8 where $R_1 = \infty$ and $R_2 = 0$. The resulting output should show a linear slope when compared to the input step. The results should closely mimic the plots illustrated in Figure 4.9.

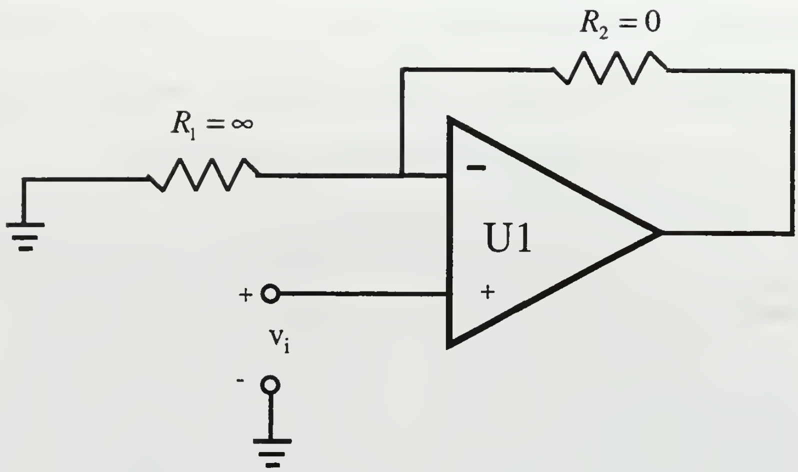



**Figure 4.8: Non-Inverting Configuration**

The following derivation shows mathematically how a step input can uncover slew-rate in an OP AMP [5]. The amplifier's closed-loop transfer function may be expressed by

$$\frac{V_o(s)}{V_i(s)} = \frac{1 + R_2/R_1}{1 + \dfrac{s}{\omega_t / \left(1 + R_2/R_1\right)}} \qquad \text{(Eq. 4.5)}$$

where (Eq. 4.5) is a non-inverting amplifier configuration. Upon setting $R_2=0$ and $R_1=\infty$, the unity gain follower circuit is obtained and the above equation reduces to

$$\frac{V_o(s)}{V_i(s)} = \frac{1}{1 + \dfrac{s}{\omega_t}} \qquad \text{(Eq. 4.6)}$$

The output response, given a step input, is given by the following equation.

$$v_o(t) = V\left(1 - e^{-t/\tau}\right) \qquad \text{(Eq. 4.7)}$$

With $\tau = 1/\omega_t$, Figure 4.9 illustrates the anticipated results.

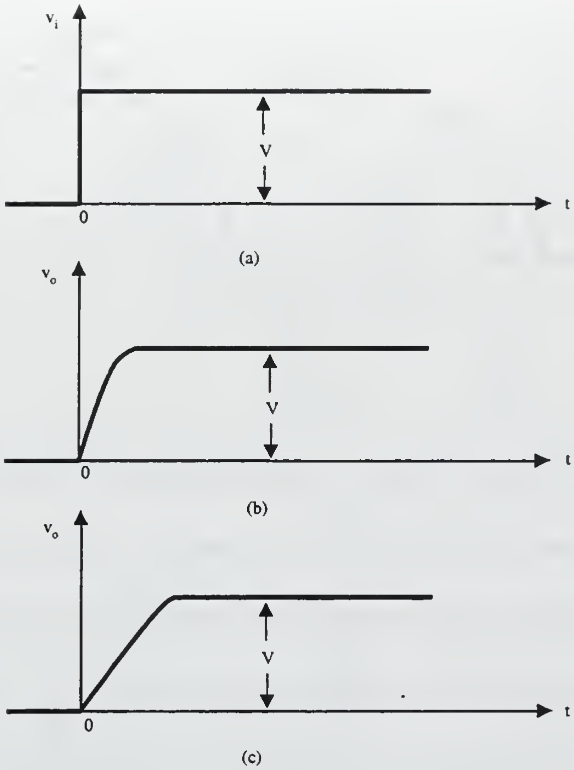



**Figure 4.9: Slew Rate With Step Input A) Step Input B) Output With $V_i$ Small C) Output With $V_i$ Large**

Slew-rate limiting caused from sinusoidal inputs is also a problem for OP AMPs. Using the unity-gain follower configuration from before and applying a sinusoidal input given by

$$v_I = \hat{V}_i \sin \omega t \,, \qquad \text{(Eq. 4.8)}$$

we obtain the derivative of the input signal as

$$\frac{dv_I}{dt} = \omega \hat{V}_i \cos \omega t \,. \qquad \text{(Eq. 4.9)}$$

When the maximum amplitude of the derivative of the input signal, $\omega \hat{V}_i$, exceeds the OP AMPs slew-rate it will produce a distortion in the output as shown in Figure 4.10.

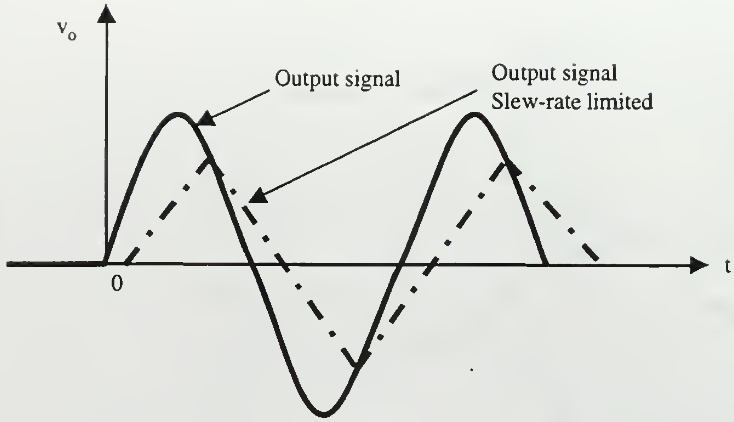



**Figure 4.10: Slew Rate With Sinusoidal Input**

Internal amplifier saturation effects are one cause of slew-rate limiting, which will ultimately determine the high-frequency operation of the OP AMP. The slew-rate test was performed in Spice with the circuit schematic illustrated in Figure 4.11. The observed slew rate was compared for several OP AMPs and the results are included in Table 4.1. [5, 13]

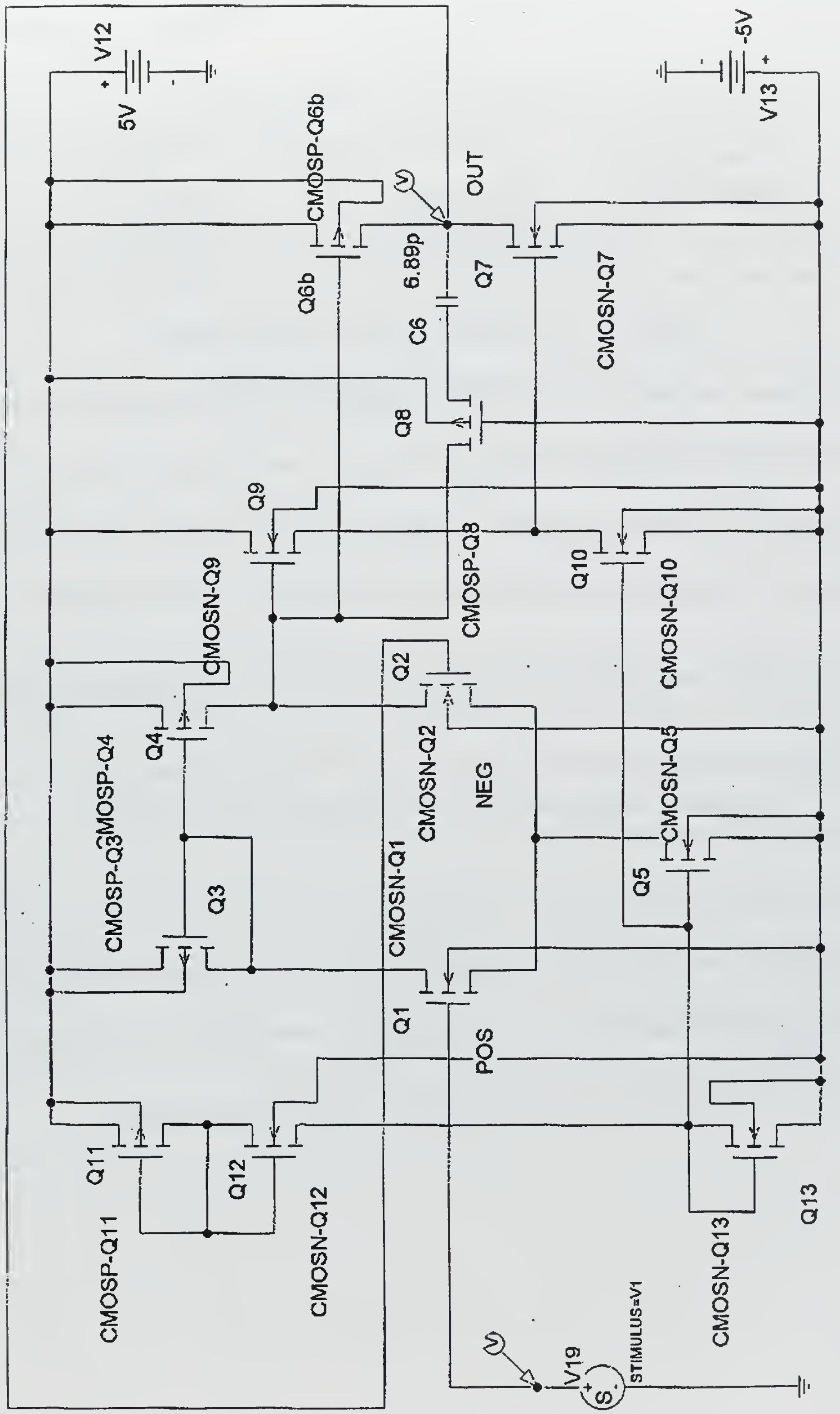



**Figure 4.11: Spice Unity-Gain Simulation**

| Type of Test | OP AMP | Results |
|---|---|---|
| Slew Rate Rising Edge | LF411ACN | 12.81V/usec |
| | Silvernagle | 3.85V/usec |
| | 10101 BPC (741) | 1.26V/usec |

**Table 4.1: Test Results For Slew Rate Limiting**

The next simulation performed with Spice was the gain band-width-product test. The simulation in Spice was configured as detailed in Figure 4.6 with an input sinusoid of .1mV at 100 Hz. Using the AC sweep function from 10 Hz to 1 MHz with 100 step size, the gain band-width-product was then plotted using the add trace feature and with the gain = $dB\left( {}^{V_o}\!/\!_{V_i} \right)$. The gain band-width-product of the Silvernagle OP AMP is shown in Figure 4.12. The results from testing the Silvernagle and other OP AMPs are listed in Table 4.2. The Silvernagle OP AMP compared favorably with the other commercial OP AMPs. [8]

It was determined as the result of testing that the Silvernagle OP AMP outperformed the 741 OP AMP in both slew rate and unity gain-band-width while complexity remained the same. Therefore, the Silvernagle OP AMP was chosen as a suitable choice for integration. The next chapter details the design of the programmable GIC filter.

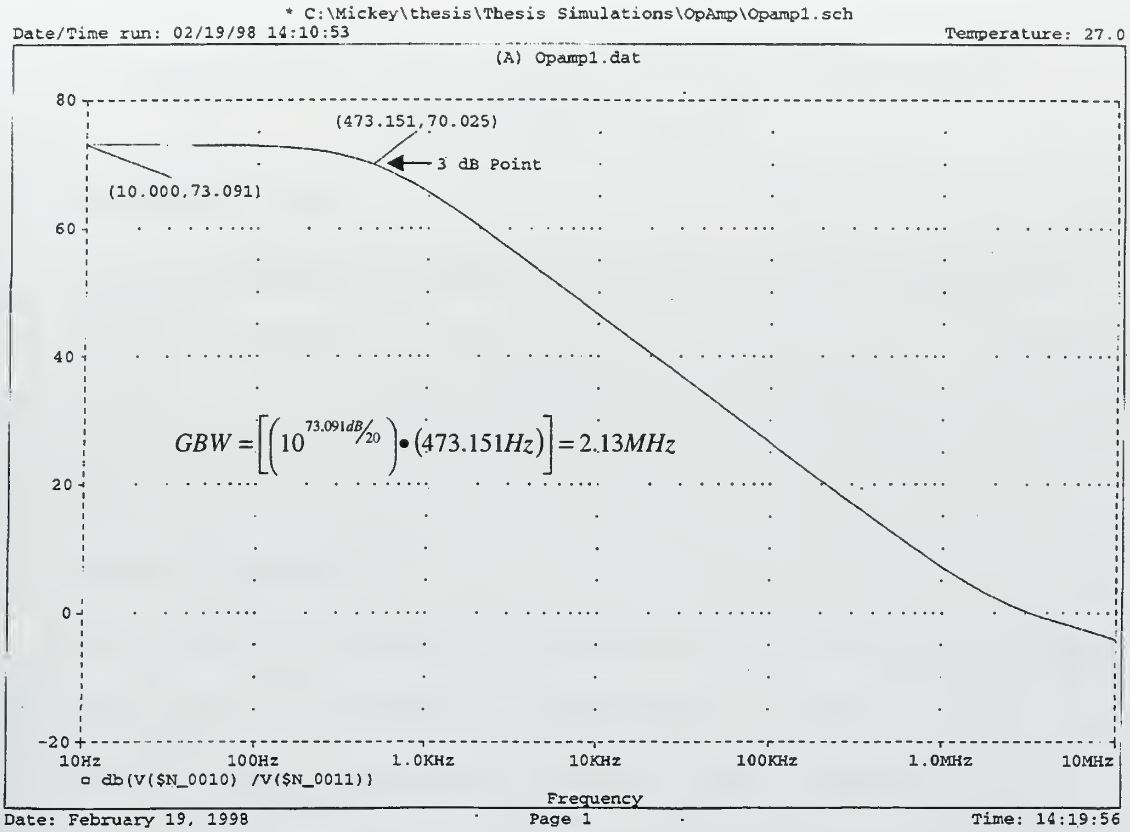



**Figure 4.12: Silvernagle Opamp Gain Bandwidth Product**

| Type of Test | OP AMP | |
|---|---|---|
| Gain Band-width Product | LF411ACN | 7.15 MHz |
| | Silvernagle | 2.13 MHz, $f_M = 471.72Hz$ |
| | 10101 BPC | 0.9 MHz |

**Table 4.2: Test Results For Gain Bandwidth Product**

# V. DESIGNING THE GENERALIZED IMMITTANCE CONVERTER FILTER

## A. INTRODUCTION

This research project has two goals. The first goal is to conduct simulations and build a programmable switched capacitor GIC filter on a wire-wrap board for testing. The second goal is to apply the knowledge gained from testing to enable integration of the filter onto a chip.

## B. PROGRAMMABILITY

One of the many advantages of switched capacitor filters is the ease with which they can be programmed to perform different functions. However, in order to completely understand the advantage offered by switched capacitor filters, the following several concepts must first be examined. The center frequency and quality factor for the GIC filter are given by (Eq. 5.1) and (Eq. 5.2):

$$\omega_p = \frac{G}{C} \qquad \text{(Eq. 5.1)}$$

$$Q_p = \frac{G}{G_q} \qquad \text{(Eq. 5.2)}$$

where $G$ is the bilinear switched capacitor admittance, $G_q$ is the quality capacitor admittance, and C is referred to as the frequency capacitor. These quantities are interrelated by

$$G = \frac{4C}{\tau} = \frac{4C_r}{T} \qquad \text{(Eq. 5.3)}$$

$$G_q = \frac{4C_{qr}}{T} \qquad \text{(Eq. 5.4)}$$

$$\omega_p = \frac{4C_r}{CT} \qquad \text{(Eq. 5.5)}$$

$$Q_p = \frac{4C_r T}{4C_{qr} T} = \frac{C_r}{C_{qr}} \qquad \text{(Eq. 5.6)}$$

$$\omega_p = 2\pi f_p = \frac{4C_r}{CT} \qquad \text{(Eq. 5.7)}$$

$$f_p = \frac{0.6366 C_r}{C} f \qquad \text{(Eq. 5.8)}$$

By adjusting the ratio of the three separate capacitances, $C_{qr}$, $C_r$ and $C$, the designer has the ability to adjust the quality factor $(Q_p)$ of the circuit, the corner frequency $(f_p)$ and even the filter type.

## C. PROGRAMMABLE FILTER TOPOLOGY

The intended design must be capable of realizing the four filter types: high-pass, low-pass, band-pass and notch. A proposed control scheme for this design uses a two-bit signal, shown in Figure 5.1. The programmable GIC control circuits used an eight-switch DIP package for switches $S_1$ through $S_8$. The desired filter type is set by the particular switch combination.

To realize the four topologies of the GIC filter shown in Figure 5.2, the admittances must be replaced with the discrete values found in Table 5.1. These components consist of admittance G, admittance $G_q$, and capacitor admittance C. The digital logic controls the placement of the components through the use of digital Quad Bilateral Switches (CD4066BC). The components that make up the digital logic are NAND gates (CD4011BCN) and inverters (CD4049CN).

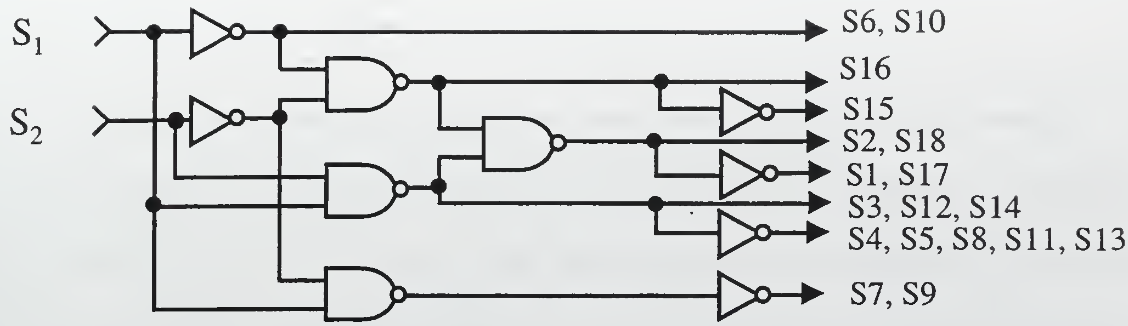



**Figure 5.1: Digital Circuit Topology**

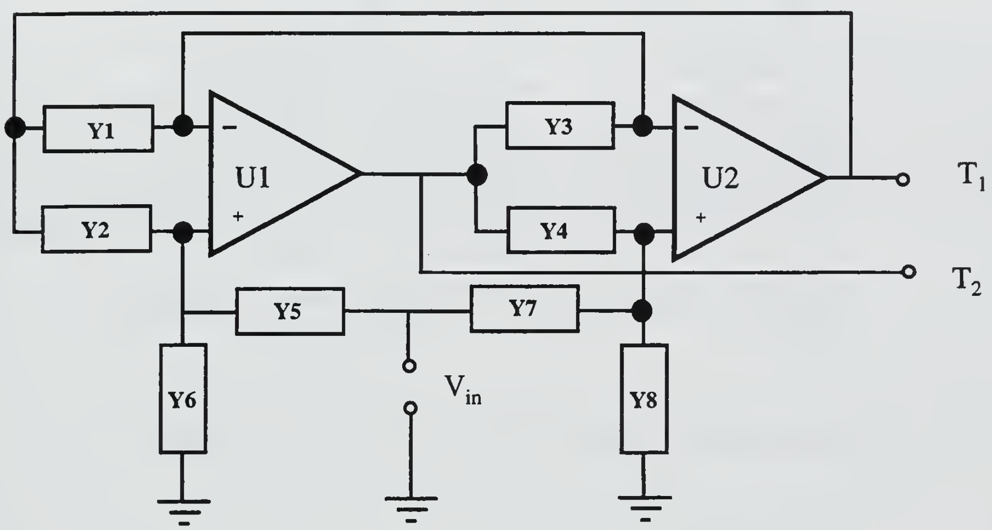



**Figure 5.2: Generalized Immittance Converter**

| Filter Type | Y1 | Y2 | Y3 | Y4 | Y5 | Y6 | Y7 | Y8 |
|---|---|---|---|---|---|---|---|---|
| Lowpass | G | C | $C+G/Q_P$ | G | G | 0 | O | G |
| Highpass | G | G | C | G | 0 | G | C | $G/Q_P$ |
| Bandpass | G | G | C | G | 0 | G | $G/Q_P$ | C |
| Notch | G | G | C | G | G | 0 | C | $G/Q_P$ |

**Table 5.1: GIC Filter Admittance Values**

Figure 5.3 shows that there are 18 switches to control [11, 14]. These 18 digital switches can be configured in different arrangements to realize the four-desired filter types. Given the proper digital logic, the four different filter topologies are obtainable through only 2-bits of information. The active switch positions for each topology are shown in Table 5.2. The data sheets for all of these components are listed in Appendix A.

| $S_1$ | $S_2$ | Topology | Active Switches | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | Notch Filter | S2 | S3 | S6 | S10 | S12 | S14 | S15 | S18 |
| 0 | 1 | High-Pass Filter | S1 | S3 | S6 | S10 | S12 | S14 | S16 | S17 |
| 1 | 0 | Band-Pass Filter | S1 | S3 | S7 | S9 | S12 | S14 | S16 | S17 |
| 1 | 1 | Low-Pass Filter | S2 | S4 | S5 | S8 | S11 | S13 | S16 | S18 |

**Table 5.2: Truth Table For Programmable Topology**

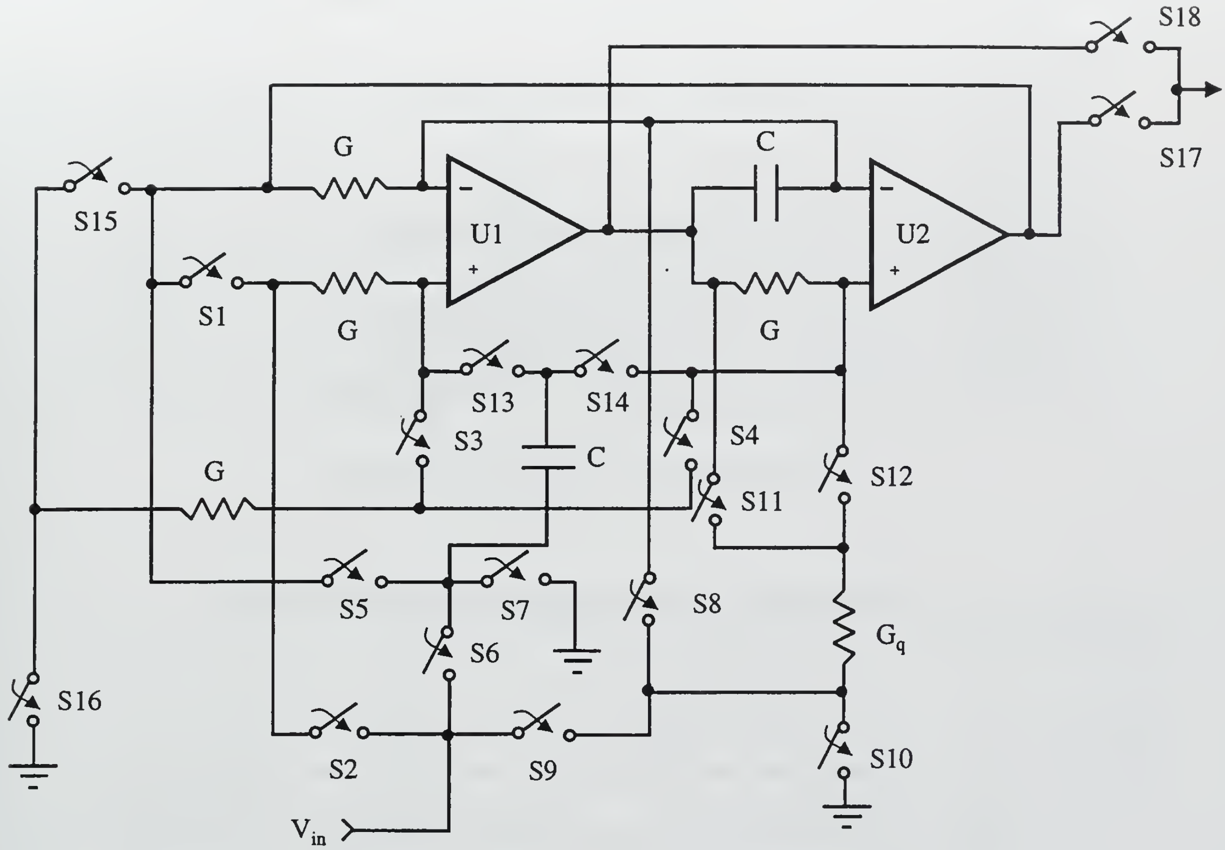



**Figure 5.3: GIC Filter With Programmable Topology**

## D. PROGRAMMABLE POLE FREQUENCY TOPOLOGY

Programming the filter pole frequency was accomplished by using the circuit shown in Figure 5.4. Using a three-bit control signal, implemented with DIP switches $S_6$, $S_7$, and $S_8$, the designer is able to control six digital switches that provide up to eight separate pole frequencies. As demonstrated in Figure 5.5 each switch, $S_6$, $S_7$, and $S_8$ , activates two digital switches simultaneously. The DIP switches directly control a bank of parallel connected capacitors. The value $C_f$ represents a unit capacitance of 3000 pF where $2C_f$ and $4C_f$ represent 6000 pF and 12000 pF, respectively. The digital switches are realized through the

of Figure 5.6 documents the entire circuit. The data sheets for all components are in Appendix D.

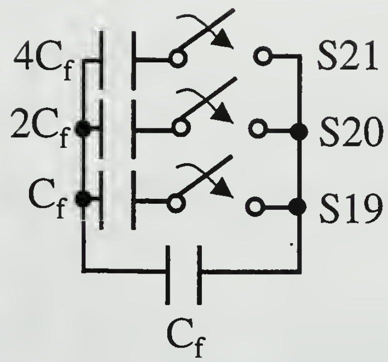



**Figure 5.4: Capacitor Network For Pole Frequency**

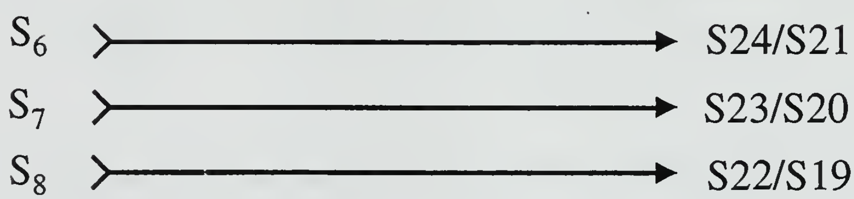



**Figure 5.5: Digital Logic Circuit for Pole Frequency**

The DIP switch position and corresponding pole frequency are shown in Table 5.2. Because of the warping effect described in chapter three the clock frequency should be approximately 10 times the pole corner frequency, but due to limitations encountered with the digital switches on the wire-wrap board 100 kHz was the highest clock frequency which provided adequate results. The results anticipated from the fabricated semiconductor chip should allow the clock frequency to be > 1 MHz. [11, 14]

| $S_6$ | $S_7$ | $S_8$ | Active Switches | Capacitance | Frequency |
|---|---|---|---|---|---|
| 0 | 0 | 0 | None | C = 3nF | 90.00 kHz |
| 0 | 0 | 1 | S19, S22 | 2C = 6nF | 51.60 kHz |
| 0 | 1 | 0 | S20, S23 | 3C = 9nF | 35.40 kHz |
| 0 | 1 | 1 | S19, S20, S22, S23 | 4C = 12nF | 26.55 kHz |
| 1 | 0 | 0 | S21, S24 | 5C = 15nF | 22.80 kHz |
| 1 | 0 | 1 | S19, S21, S22, S24 | 6C = 18nF | 18.45 kHz |
| 1 | 1 | 0 | S20, S21, S23, S24 | 7C = 21nF | 15.60 kHz |
| 1 | 1 | 1 | S19, S20, S21, S22, S23, S24 | 8C = 24nF | 13.95 kHz |

**Table 5.3: Frequency vs. Capacitance**

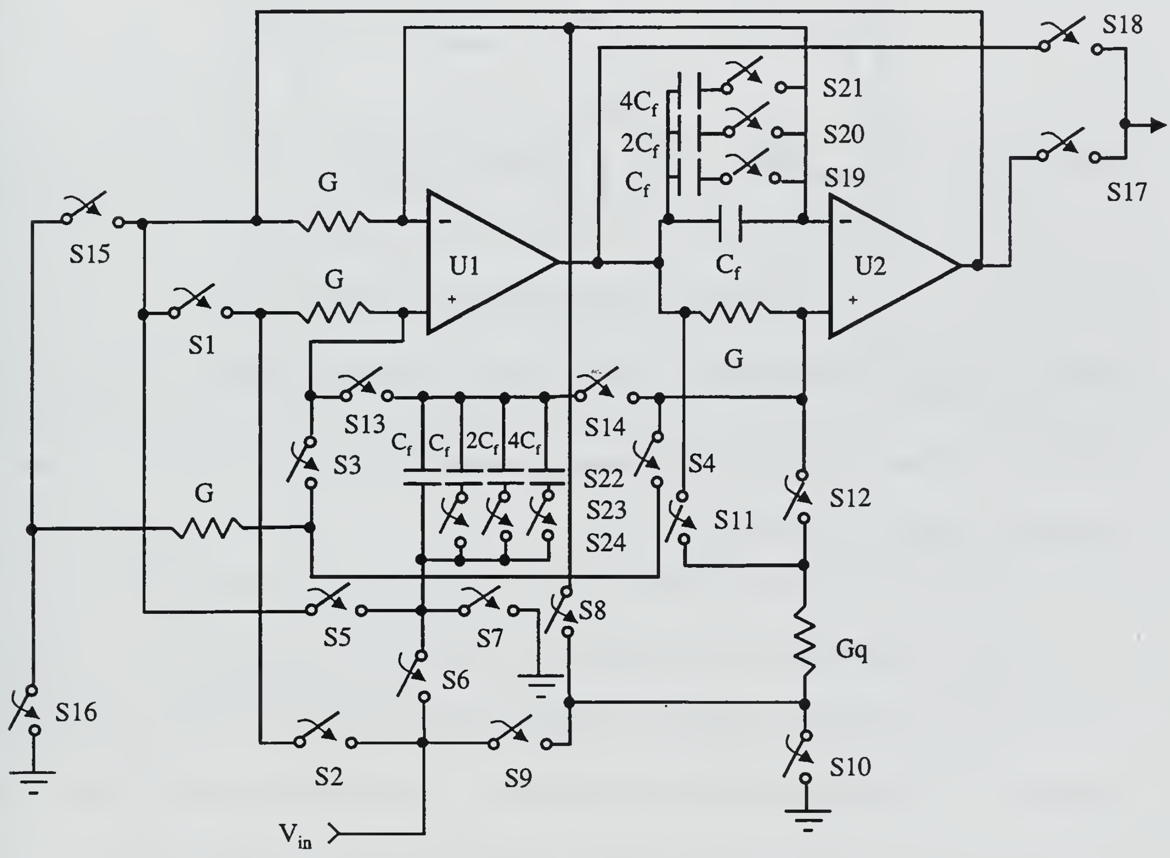



**Figure 5.6: GIC Filter With Programmable Topology And Pole Frequency**

## E. PROGRAMMABLE POLE QUALITY FACTOR TOPOLOGY

The pole quality factor is programmed by a three-bit control signal from DIP switches $S_3$, $S_4$, and $S_5$. This allows the selection of eight different pole quality factors over the range of $0.8 \leq Q_p \leq 5.0$. The pole quality factor circuit is realized through the use of five unit capacitors $(C_q)$ and a network of switches and digital control logic (shown in Figure 5.7). A decision was made to stay with the stated small change in pole

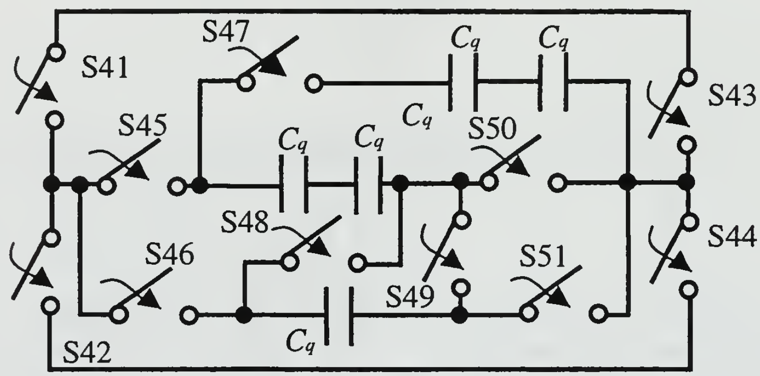



**Figure 5.7: Network For Quality Factor**

quality factor, $Q_p$, to minimize the amount of digital control logic as shown in Figure 5.8. It should be noted that by adding levels of selectivity to the circuit, the maximum pole quality factor for the circuit is not increased.

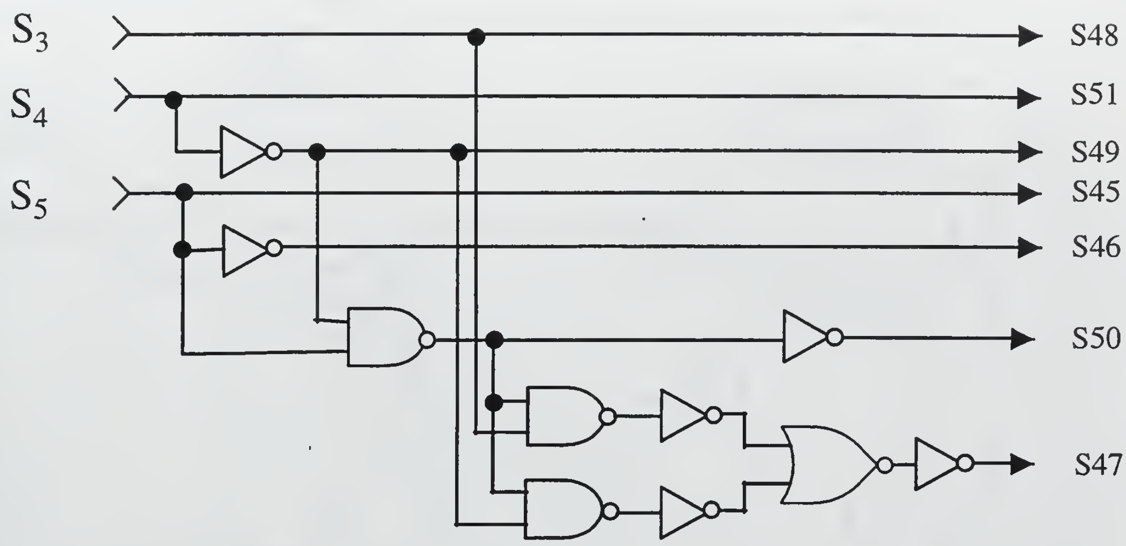



**Figure 5.8: Digital Logic Circuit For Quality Factor**

| The Q | $S_3$ | $S_4$ | $S_5$ | S45 | S46 | S47 | S48 | S49 | S50 | S51 |
|---|---|---|---|---|---|---|---|---|---|---|
| 0.8 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 |
| 2 | 1 | 0 | 0 | 1 | 0 | 0 | X | X | 1 | 0 |
| 3 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 1 |
| 4 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | X | 0 | 0 |
| 5 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 |

**Table 5.4: Quality Factor**

The control signals are selected to provide a simplified digital logic circuit. Table 5.4 describes the state of the switches for each control signal and the resulting pole quality factor. Figure 5.9 shows a programmable GIC filter with digital switches and components that will realize the filter type, center or cutoff frequency and the quality factor. A complete and tested Programmable General Immittance Converter filter is shown in Appendix A.

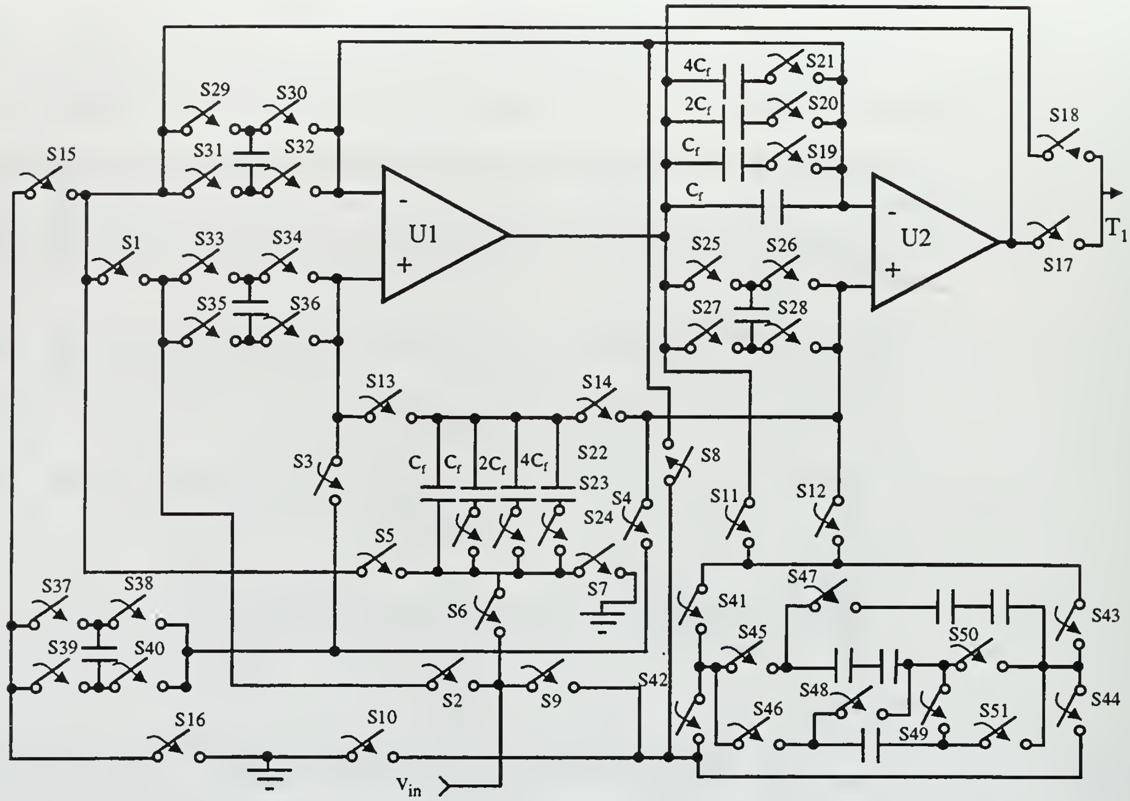



**Figure 5.9: GIC Filter With Programmable Topology, Pole Frequency And Quality Factor**

## F. CONSTRUCTING AND TESTING OF THE PROGRAMMABLE GIC CIRCUIT

The components were selected so that the circuit of Figure 5.9 could realize a second-order GIC filter with the following programmability:

- Filter Topology
- Pole Frequency
- Pole Quality Factor

As seen in the circuit layout of Appendix A, the OP AMPS used are LF411ACN and the capacitors for the bilinear and variable bilinear resistors are 3 nF. The clock speed was set for 100 kHz. Using a HP 3585B Spectrum Analyzer, two sets of output responses were

generated. The first data set is compared at different frequency values where Q=5. The second set of output responses is compared with the frequency constant (~8.8 kHz) and Q is varied. The output graphs appear as anticipated and are recorded in Appendix A. The next chapter covers the implementation of the GIC on a chip. [11, 14]

# VI. VLSI LAYOUT

## A. INTRODUCTION

The second goal of this research project was to integrate a programmable Generalized Immittance Converter (GIC) filter into a semiconductor chip. The design considerations of this chapter combine the GIC filter material discussed in Chapter II, the switched capacitors techniques introduced in Chapter III, the operational amplifier details presented in Chapter IV, the networks that achieve GIC programmability as detailed in Chapter V, and the design limitations encountered in Very Large Scale Integration (VLSI).

## B. SEMICONDUCTORS

Silicon (SI) in its pure state has a resistive property somewhat like an insulator and is essential for the Metal Oxide Silicon (MOS) process. The reason for using SI is that it is abundantly available and can be manufactured to a very high purity level. As shown in Figure 6.1 an atom of pure silicon has a total of fourteen electrons, four of which are in the outer valence shell. Pure silicon is formed by a process termed covalent bonding.

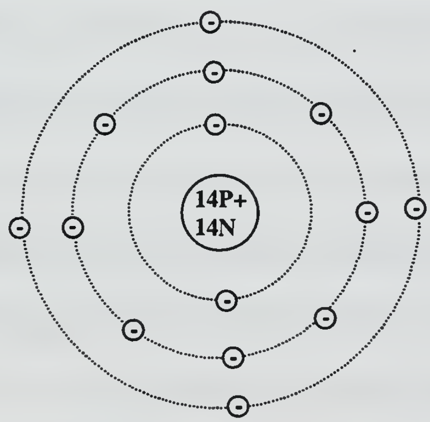



**Figure 6.1: Bohr concept of an Atom of Silicon**

The central silicon atom in Figure 6.2 is shown as sharing electrons from each of the four neighboring silicon atoms. Each of the four neighboring atoms, in turn, is sharing one of the electrons of the central atom's valence shell for bonding purposes. Thus, none of the atoms exclusively have eight electrons in its valence shell but shares electrons with neighboring atoms. The process of sharing electrons to fill the outer valence shell is termed covalent bonding.

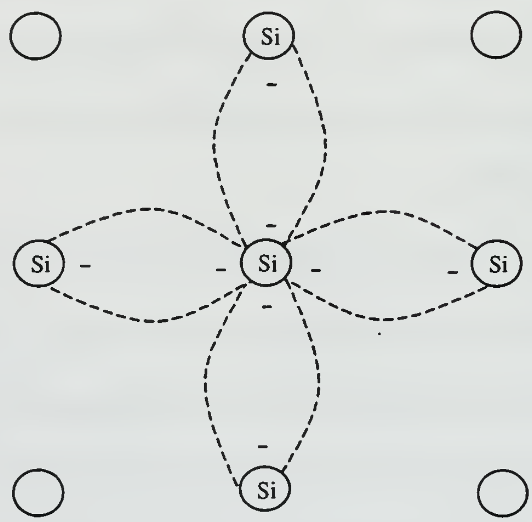



**Figure 6.2: Depiction of Covalent Bonding in Silicon Atoms**

A valence electron in a neighboring atom can leave its covalent bond quite easily to fill a hole. When the free electron leaves its bond, a hole is left behind. The hole has effectively moved in the opposite direction. This process can continue, with the holes moving to the right as electrons progress to the left. Thus, this mechanism does not involve the movement of positive charge or holes only. The charge motion, or current, in pure silicon is the sum of the free electron flow and the hole flow.

Pure intrinsic silicon has very low conductivity, and thus it is classified as an insulator. The conductivity can be increased significantly, making the silicon a semiconductor, by the addition of certain materials known as impurities or doping agents.

The silicon is then called extrinsic, or a doped semiconductor. The added impurities are either pentavalent (5 valence electrons) or trivalent atoms (3 valence electrons).

Phosphorus is a pentavalent material it has five electrons in its outer valence shell. When a small percentage of phosphorus is added to pure silicon, the phosphorus atoms displace some of the silicon atoms, forming the arrangement shown in Figure 6.3. Since only

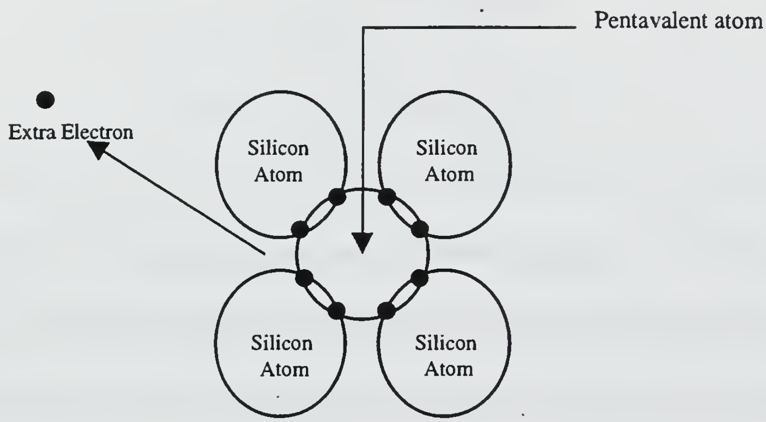



**Figure 6.3: N-Type Semiconductor**

four of the five electrons are needed for covalent bonding, one electron is donated to the crystalline structure. At room temperature, this fifth unbonded electron is easily detached from its parent atom to become a free electron. The phosphorus impurity is called a donor n-type impurity material. The atom itself is ionized, acquiring a bond positive charge that is not free to move.

The next in the process involves the addition of aluminum, a trivalent impurity, to silicon. Since there are only three electrons in the aluminum atom's valence shell, the substitution of an aluminum atom for a silicon atom leaves an incomplete bond. This bond is usually completed when a neighboring silicon atom donates an electron. The aluminum atom thus acquires a bound negative charge, and a hole is left where the electron came from as shown in Figure 6.4. Since the aluminum atom has created a hole that can accept

electrons, aluminum is known as an acceptor impurity. The aluminum impurity has caused the p-type silicon to have many more holes than free electrons.

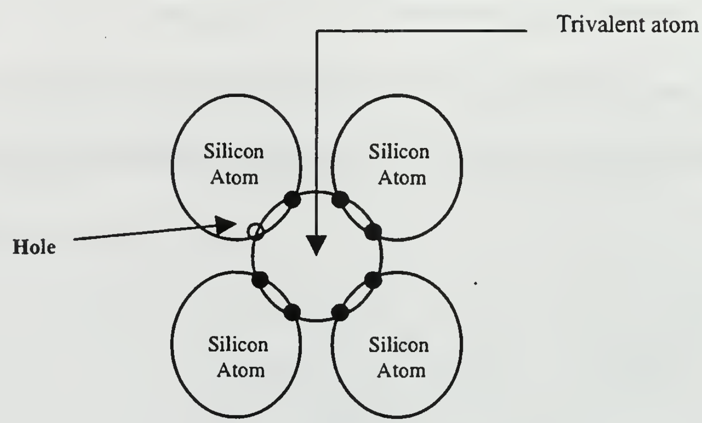



**Figure 6.4: P-Type Semiconductor**

The majority carrier in the n-type material is the electron and holes are the majority carrier for the p-type silicon. The n-type and p-type silicon materials have much greater conductivity then that of pure silicon. [6]

## C. METAL OXIDE SILICON TRANSISTORS

Layers of p-type silicon, n-type silicon, silicon dioxide (an insulator), polysilicon (doped SI) and metal creates the MOS structure. A very thin smooth layered circular wafer of p-type or n-type silicon forms the substrate (also known as bulk) structure. The substrate of a wafer and polysilicon has the same crystal structure. As a result, polysilicon can be grown in very thin smooth layers while still maintaining its structural integrity. Lacing polysilicon with metal reduces its high resistivity to create a non-uniform polysilicon. The non-uniform polysilicon is frequently used as a conductor and is used to construct gates and capacitor plates.

An N-type Metal Oxide Silicon (NMOS) transistor is illustrated in Figure 6.5. The NMOS structure consists of a moderately doped p-type silicon substrate into which two

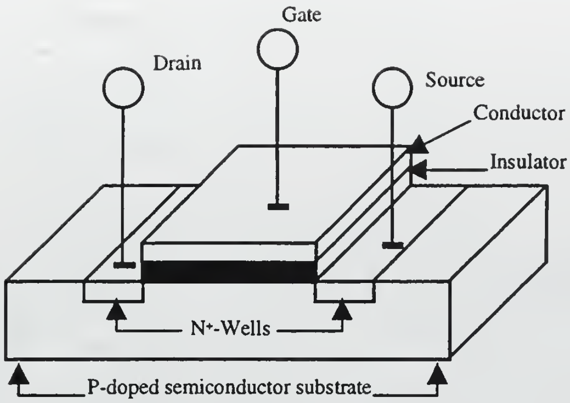



**Figure 6.5: NMOS Transistor**

heavily doped $n^+$ regions, called the source and the drain, are diffused. Between these two regions lies a narrow region of p-type substrate, called the channel, covered by a polysilicon gate. A thin layer of silicon dioxide ($SiO_2$) insulates the channel from the gate. If a positive voltage is applied between the source and the drain $(V_{ds})$, with the gate bias zero, no current will flow (only in enhancement mode devices). But if sufficient positive voltage is applied to the gate with respect to the source, current will flow from drain to source as shown in Figure 6.6.

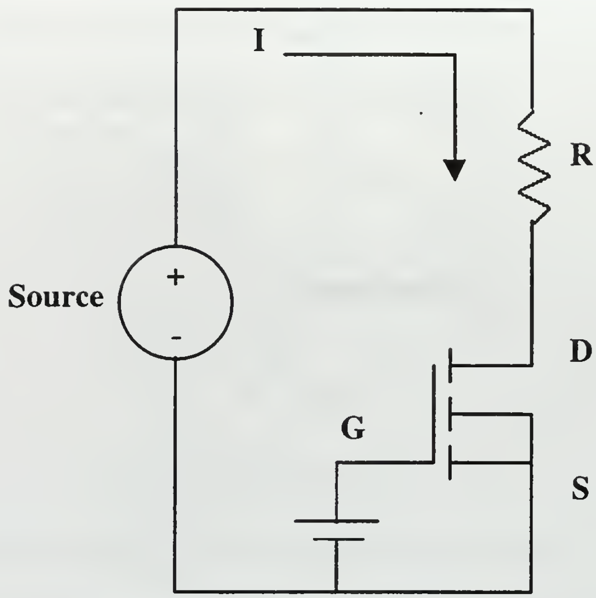



**Figure 6.6: Current Flow for an N-Channel Enhancement Mode Transistor**

A p-type Metal Oxide Silicon (PMOS) transistor is fabricated on an n-type substrate with $p^{+}$ regions for the drain and source, and hole flow for current. A PMOS transistor operates on the same principle as the NMOS except that the required voltages for $v_{GS}$ and $v_{DS}$ are negative and the threshold voltage $v_t$ is negative. The PMOS transistor is illustrated in Figure 6.7. A p-channel transistor will turn off when the gate is grounded, and a positive voltage is applied to the source. A negative gate voltage draws holes into the region below the gate, resulting in the channel changing from n-type to p-type. With this a conduction path is created between the source and drain allowing current to flow [6].

As the name implies, Complementary Metal Oxide Silicon (CMOS) technology employs MOS transistors of both polarities. Although CMOS circuits are somewhat more difficult to fabricate than NMOS, the availability of complementary devices makes possible many powerful circuit-design possibilities. A CMOS cross section is shown in Figure 6.8.

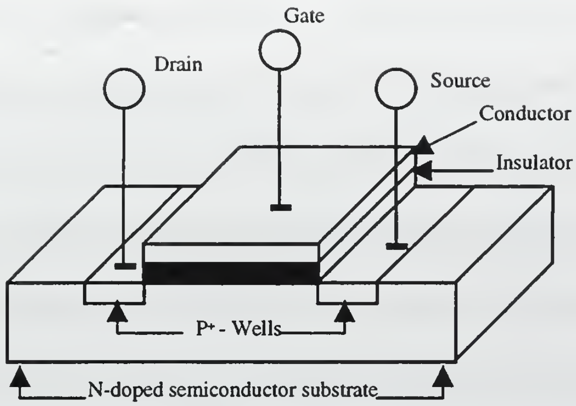



**Figure 6.7: PMOS Transistor**

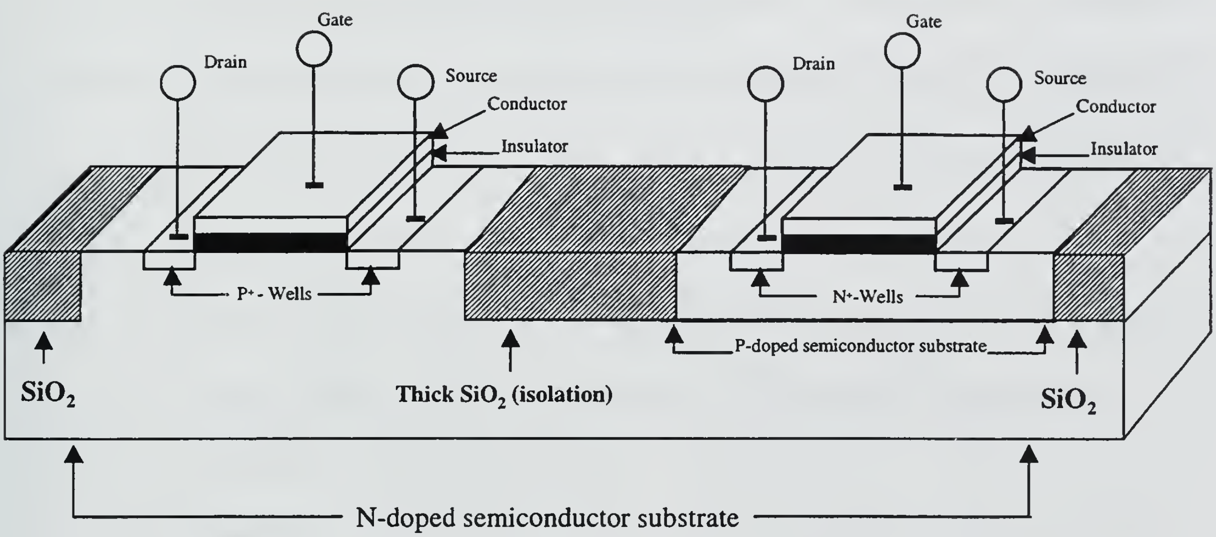



**Figure 6.8: Cross Section of a CMOS Integrated Circuit**

## D. DESIGN LIMITATIONS

A parasitic circuit effect called latchup exists in CMOS technology. At a minimum this type of effect would require a power down to reset the device, but the worst case would result in the destruction of the chip as a result of shorting the power supply lines. In earlier

manufacturing of CMOS devices, latch-up was a significant problem, but today it has been almost eliminated by following a few basic rules that are summarized in this section.

The reason latchup occurs may be explained by reviewing the CMOS inverter structure shown in Figure 6.9. The inverter is constructed with NMOS and PMOS transistors and a parasitic circuit made up of a npn-transistor, a pnp-transistor, and two resistors. Under certain conditions, the parasitic circuit looks and responds very similar to that of a Silicon Controlled Rectifier (SCR). It possesses a voltage and current characteristics that above a *"critical voltage (known as the trigger point) the circuit snaps and draws a large current while maintaining a low voltage across the terminals also know as the holding voltage"* [7]. This is obviously a short circuit. These bipolar and resistor devices are the unwanted byproducts of producing MOSFETS [7].

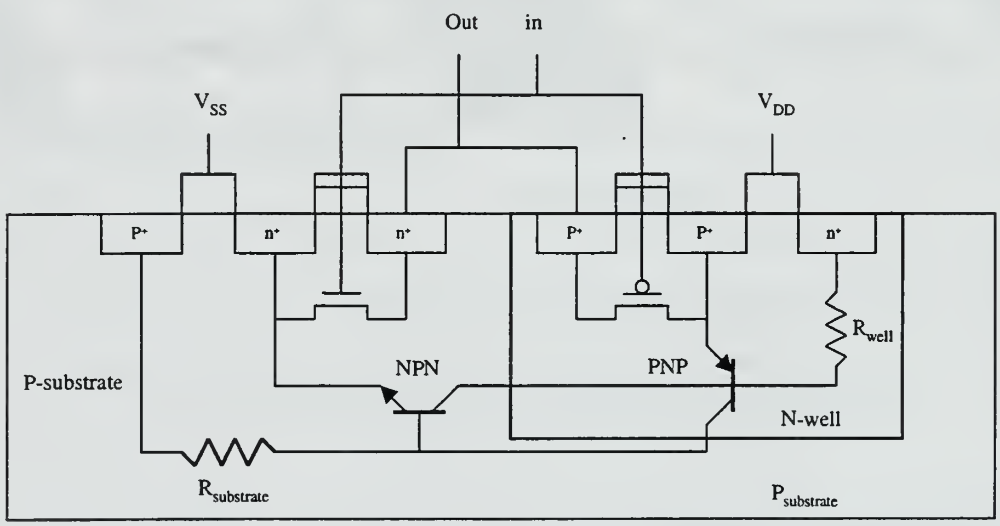


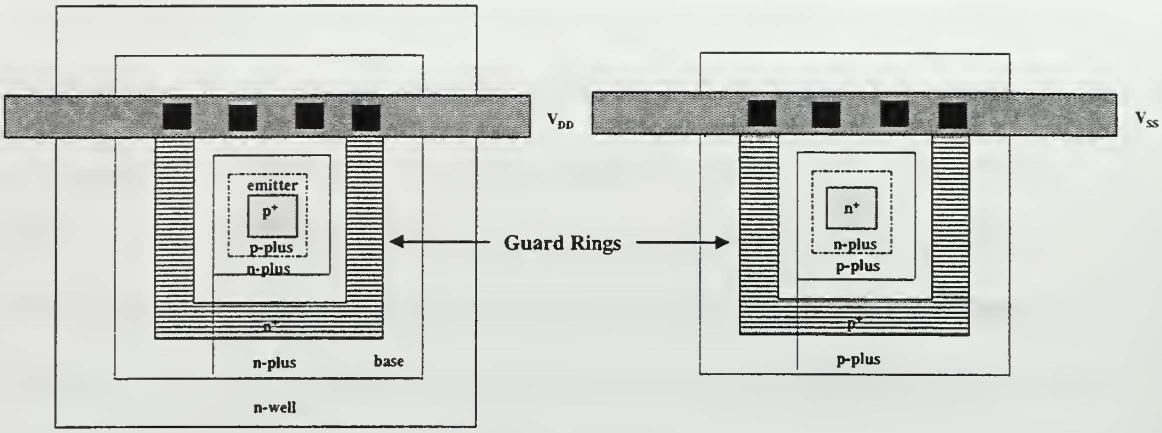

**Figure 6.9: CMOS Inverter**

The key to reducing the occurrence of latchup is the additional placement of substrate contacts, which are contacts that connect the substrate (or bulk) to the appropriate

supply source $V_{SS}$ or $V_{DD}$. Eliminating latch-up can be accomplished by designing in accordance with *Principles of CMOS VLSI Design* [7], as described below:

- Every well (either p- or n- substrate) must have a substrate contact (a contact is a physical connection) of the appropriate supply source $V_{SS}$ or $V_{DD}$.
- Every substrate contact should be connected to metal directly to a supply pad.
- Place the substrate contacts as close as possible to the source connection of the transistors. This reduces the value of $R_{substrate}$ and $R_{well}$ ($R_{substate}$ and $R_{well}$ are the byproducts of producing MOSFETS). A very conservative rule would place one substrate contact for every supply connection.
- A less conservative rule than the above places a substrate contact for every 5-10 transistors or every 25-100 $\mu$. This may be applied by grouping like transistors with a single contact or using the physical measurement of the chip in microns.
- Lay out n- and p-transistors with packing (tightly arranged) of n-devices toward $V_{SS}$ and packing of p-devices toward $V_{DD}$. Avoid structures that intertwine n- and p-devices in checkerboard styles.

Another problem is I/O latchup. A way to combat this problem is to reduce the gain of the parasitic transistors. This can be achieved through the use of guard rings. A $p^+$ guard ring is placed around a $n^+$ source/drain, while $n^+$ guard ring is placed around a $p^+$ source/drain. As depicted in Figure 6.10 guard rings act as "*dummy-collectors*" that reduce the gain of the parasitic transistors. These rings acting as collectors prevent minority carriers from effecting their respective transistor base, but minority carriers can flow underneath the




a. b.

**Figure 6.10: a). n$^+$ Guard Ring b). p$^+$ Guard Ring**

guard rings. However through the use of double guard rings, this effect can be eliminated. This technique has the disadvantage of sacrificing real estate for internal structures.

The most common place for latchup to occur is in an I/O cell that produces a large amount of current flow, such as an inverter with a heavy load. For this condition there are two ways to remove latch-up possibilities. The first approach involves a redesign to reduce the overall current flow and minimize parasitic effects. In the second approach, I/O latch-up can be eliminated or reduced if the circuit is designed in accordance with *Principles of CMOS VLSI Design* [7], as described below:

- Physically separate the n- and p-driver transistors (i.e., with the bonding pad).
- Include p$^+$ guard rings connected to $V_{SS}$ around n-transistors.
- Include n$^+$ guard rings connected to $V_{DD}$ around p-transistors.
- Source diffusion regions of the n-transistors should be placed so that they lie along equipotential lines when current flows between $V_{SS}$ and the p-wells; that is, source fingers should be perpendicular to the dominant direction of current flow

rather than parallel to it. This reduces the possibility of latchup through the n-transistor source due to an effect called "field aiding" (the effects of parallel metal supply lines contributing a parasitic effect).

- Shorting n-transistor source regions to the substrate and the p-transistor source regions to the n-well with metallization along their entire lengths will aid in preventing either of the transistor junctions from becoming forward-biased and hence reduces the contribution to latchup from these components.
- The spacing between the n-well $n^+$ and the p-transistor source contact should be kept to a minimum. This allows minority carriers near the parasitic pnp-transistor emitter-base junction to be collected and reduces $R_{well}$. The rules for the 1 $\mu$ process (a process that the smallest transistor size can be 1 $\mu$) suggest one contact for every 10 $\mu$ -50 $\mu$ (length).
- The separation between the substrate $p^+$ and the n-transistor source contact should be minimized. This results in reduced minority carrier concentration near the npn-emitter-base junction. Similar spacing to those suggested above applies for processes in the 1 $\mu$ range.

Following the above rules should eliminate all possible latchup effects in a CMOS design.

## E. CADENCE DESIGN TOOLS

When creating a new design using the Cadence software, there are seven steps that must be completed to ensure a working circuit prior to fabrication. These seven step are listed below:

- Creating a new library

- Creating a cell category
- Creating a new design using Composer
- Creating a symbol with Composer
- Simulating the design with Spectre
- Creating the layout with Virtuoso
- Simulating the layout with Spectre

Tutorials and user manuals are available to supplement the details of these individual steps [15]. Various details on the use of Cadence in circuit design are also available in Ref. [7].

## F. VLSI LAYOUT

The floor-plan and pad assignment for the two programmable GIC filters and two OP AMPS are illustrated in Figure 6.11 while the VLSI layout for the 40 pin chip is shown in Figure 6.12. The two programmable GIC filters that are arranged in Figure 6.12 show cell #1 located at the top of the pad ring and cell #2 located at the bottom. The two OP AMP cell is centered between the two programmable filters. The filters were broken down into separate sections, to help the pictorial location of the separate cells.

The following list contains sections of the programmable GIC filter cell:

- Two Phase Clock
- Bilinear Switched Capacitor
- Quality Logic
- Frequency Logic
- Topology Logic
- Variable Bilateral #1
- Variable Bilateral #2
- Opamp #1

- Opamp #2

The higher operating frequency cells and digital logic cells were located as far away from the analog sections as possible. This arrangement helps to reduce any possibility of latch-up. The final layout was submitted to MOSIS for fabrication. The layout for each cell and cell components are located in Appendix B. The final chapter will discuss the conclusions and recommendations found during this research effort.

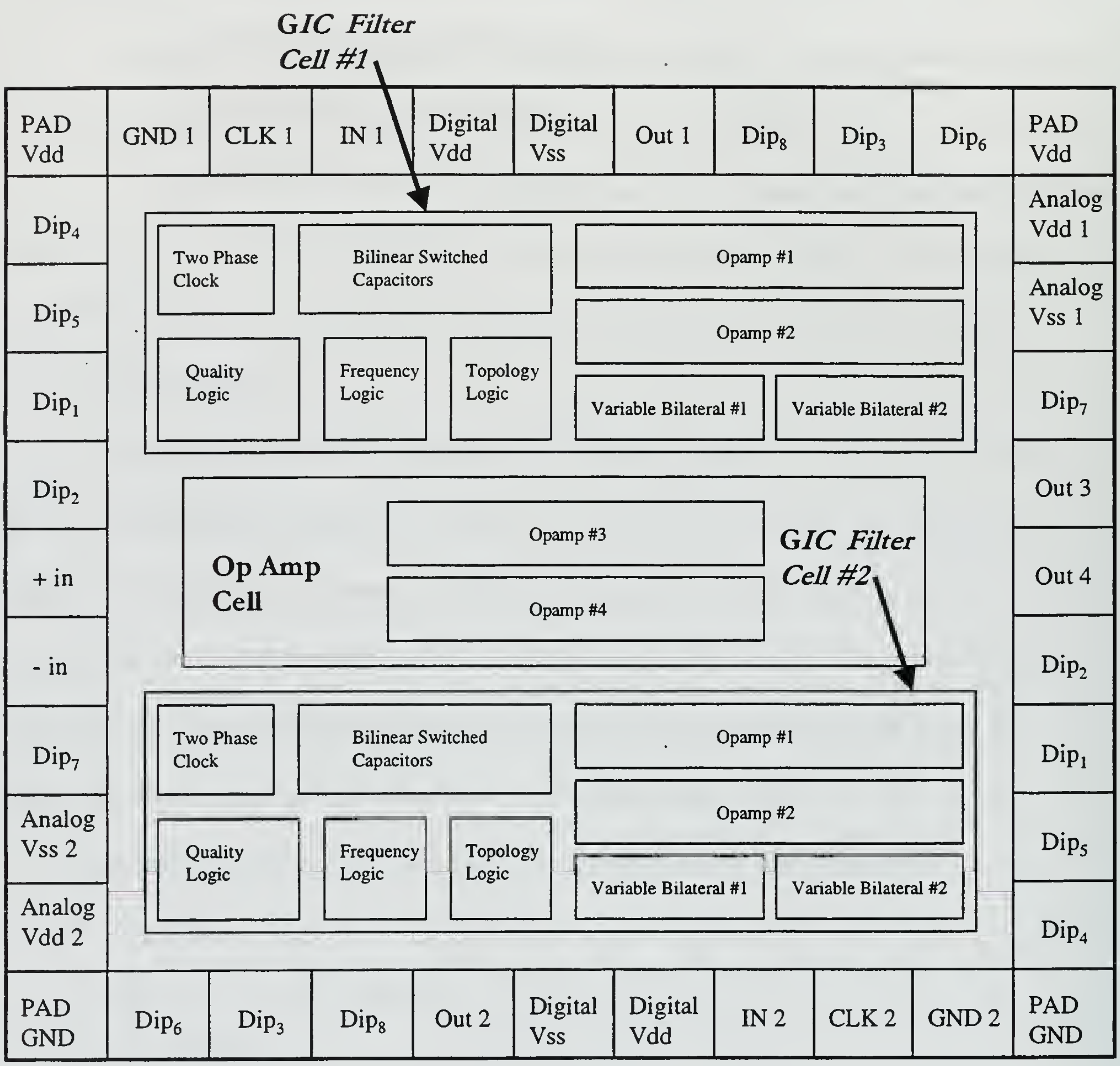



**Figure 6.11: Floor Plan of a Two-Stage Programmable GIC Filter with Two OP AMPS**

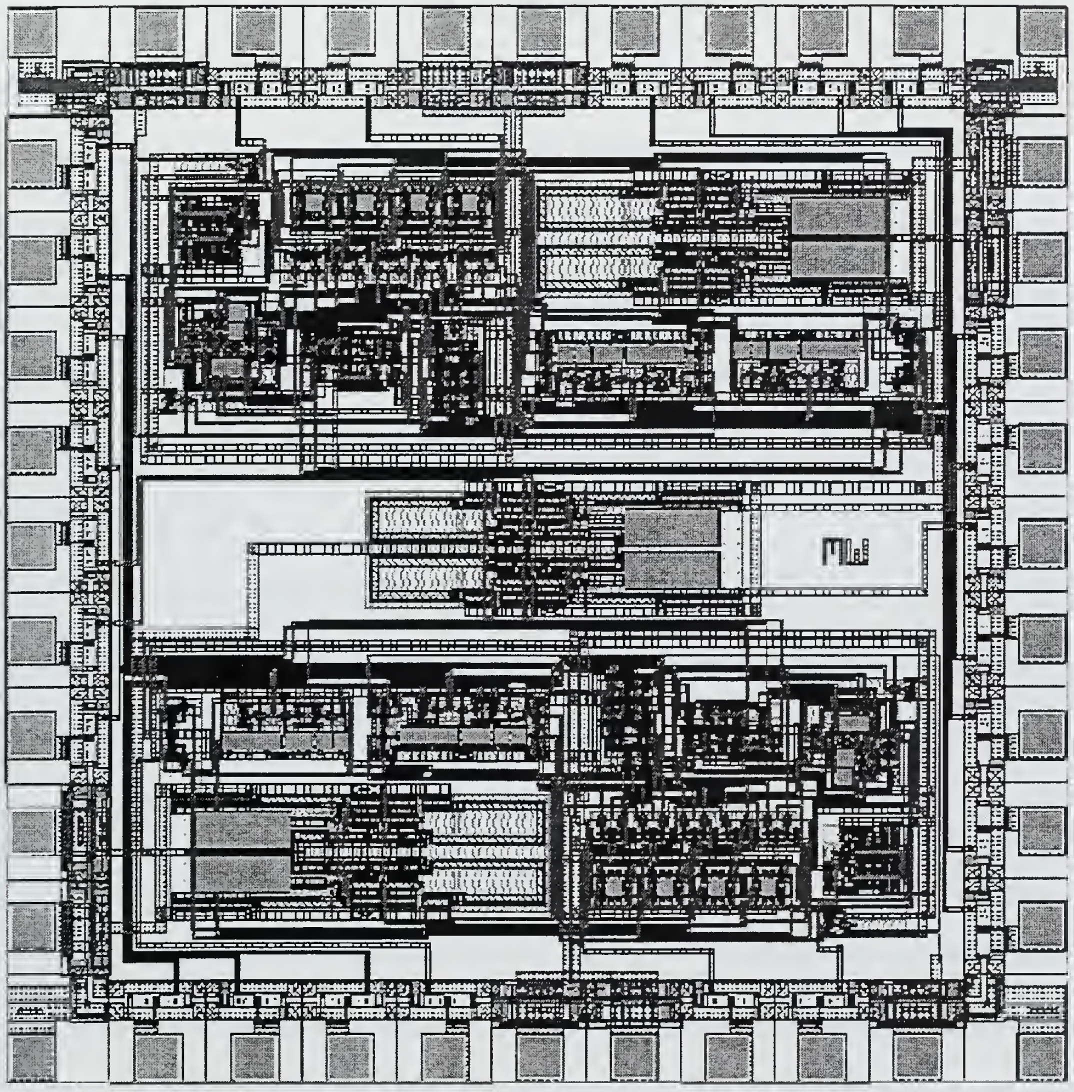


Figure 6.12: VLSI layout of the Two-Stage Programmable GIC Filter with Two OP AMPS

# VII. CONCLUSIONS AND RECOMMENDATIONS

## A. CONCLUSIONS

The goals of this research were to design and implement a VLSI, digitally programmable, two-stage, Generalized Immittance Converter Filter using the Cadence design tool software package. This programmable filter product will be very beneficial in applications involving signal processing, controls and communications systems. Once fabricated, these semiconductor chips can be used for studying the effects of stray capacitance on the integrated circuit design. The testing of the filters can add to the research data and help further the use of bilinear-switched capacitors in integrated filter designs. Testing these microchips can also demonstrate bandwidth limitations of an integrated programmable GIC filter.

It was mathematically shown that a circuit built with resistors could be transformed into a new circuit using switched capacitors. Also, through the use of digital logic, the programmability of the GIC filter was realized. Once the circuit was constructed on a wire-wrap board and tested, it re-enforced the programmability concept of the GIC filter. Through the use of Spice simulations, Cadence simulations and then finally a working programmable GIC filter on a wire-wrap board, viability of the design was proved. The final proof of concept can be achieved once the filter is fabricated on a microchip and tested.

The Cadence design tool software package was found to have several advantages over the older software package MAGIC; however, the learning curve was steep and significant amount of time was required to learn to use it. Cadence is a complete design tool software package. It has its own simulation software integrated into the Virtuoso Layout Editor. Virtuoso provides for a hierarchical integrated circuit (IC) layout that can also

provide a verification environment that supports all IC design techniques. After laying out the design, Cadence can simulate the layout using the same file that was used on the schematic. This is done with Spectre, the circuit simulator that uses direct methods to simulate analog and digital circuits. The ability to simulate either schematic or layout in the same software package is an excellent feature. It gives the designer the ability to compare the layout to the schematic prior to fabrication.

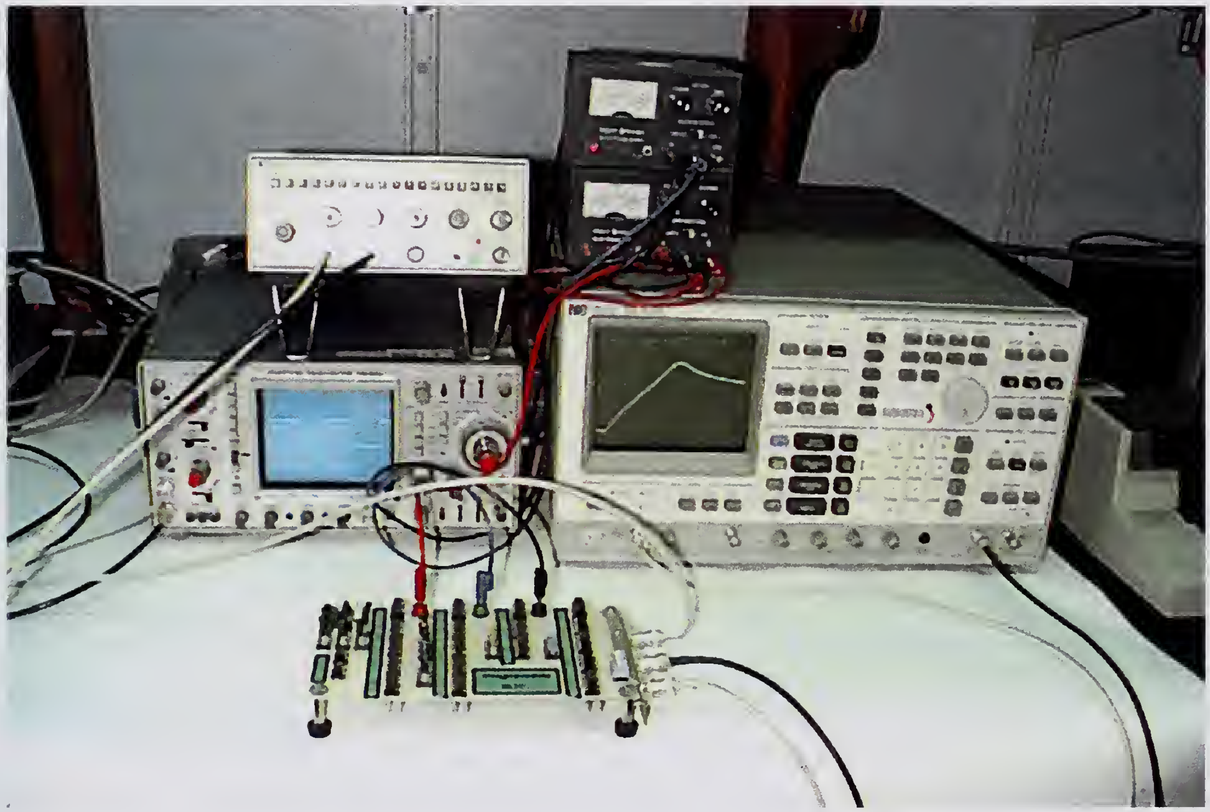
## B. RECOMMENDATIONS

The design and simulation using the Cadence software package of the stray insensitive GIC circuit is the initial step in the development of an analog/digital circuit on a microchip. Increasing the knowledge base for the Cadence software package through the use of dedicated classroom instruction will greatly benefit the research and development of the GIC filter design. Adding one or two labs (Analog/digital simulations using Cadence software) to an already long but outstanding course, EC4870, will greatly enhance a designer's ability to achieve fabrication success.

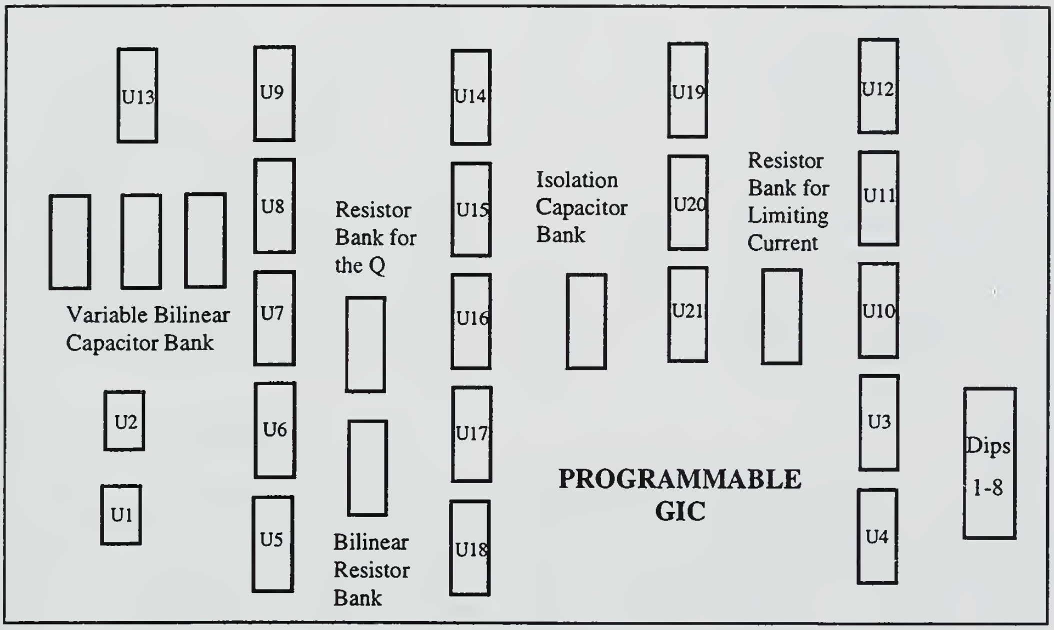
# APPENDIX A. PROGRAMMABLE GIC FILTER

## A. PROGRAMMABLE GIC

### 1. Operational GIC



## 2. Programmable Gic Circuit Board Layout




**U1, U2** - LF411ACN Operational Amplifiers

**U3, U11** - CD4011 Quad Two Input NAND Gate

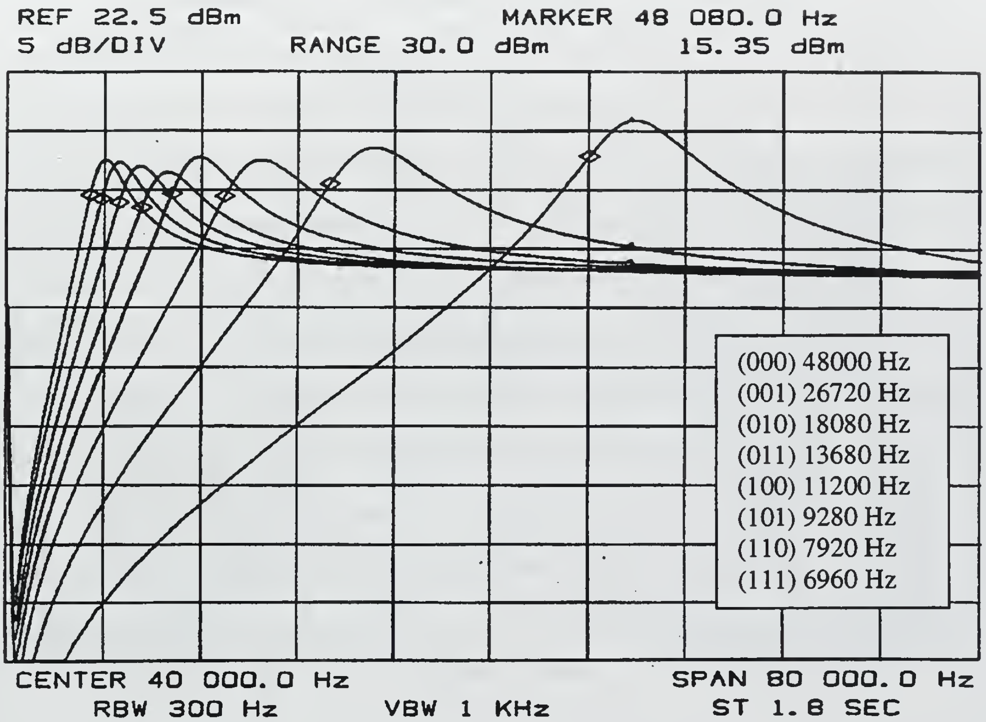
**U4, U10, U21** - CD4049CN Hex Inverting Buffer

**U12** - CD4001BEX Quad Two Input Nor Gate

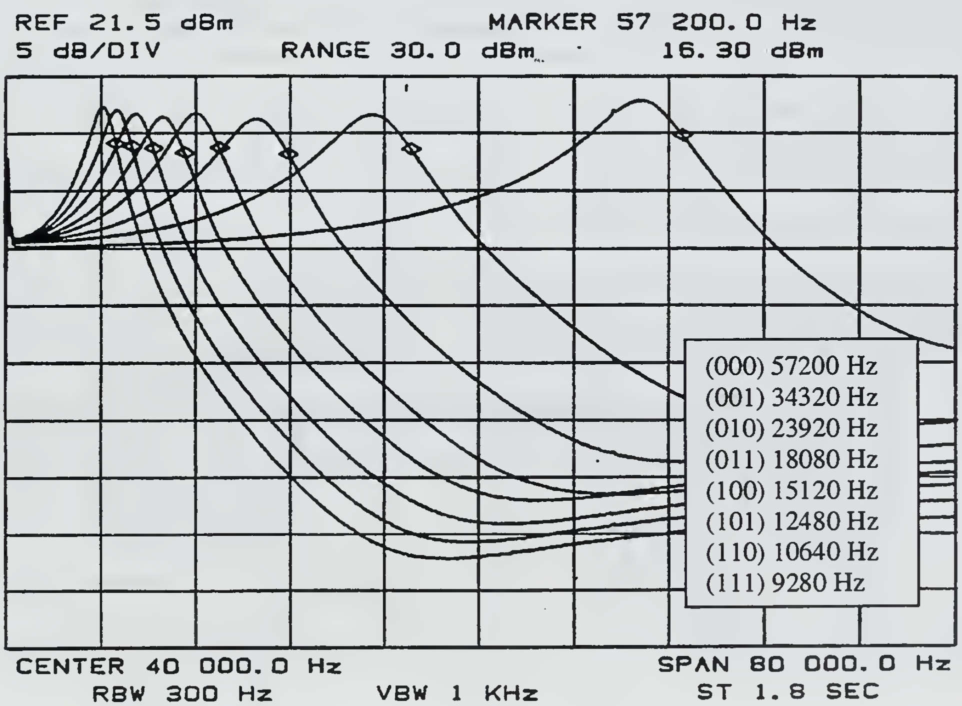
**U5, U6, U7, U8, U9, U13, U14, U16, U16, U17, U18, U19, U20** - Quad Bilateral Switch

## B. GIC OUTPUT GRAPHS WITH Q=5

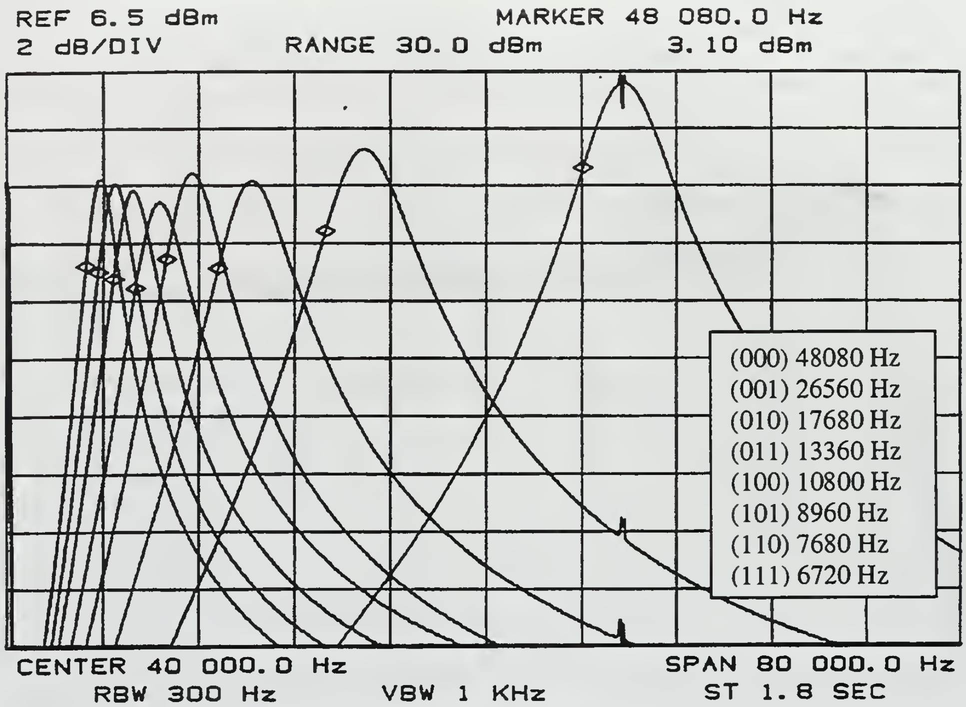
### 1. High Pass Filter



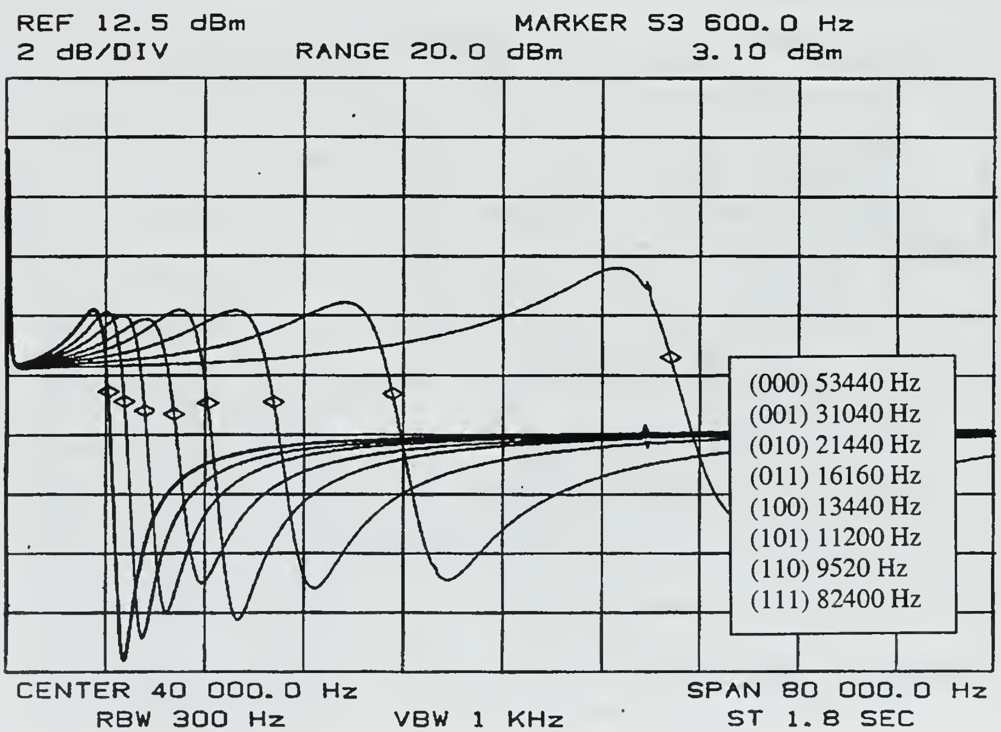

### 2. Low Pass Filter



3. Band Pass Filter

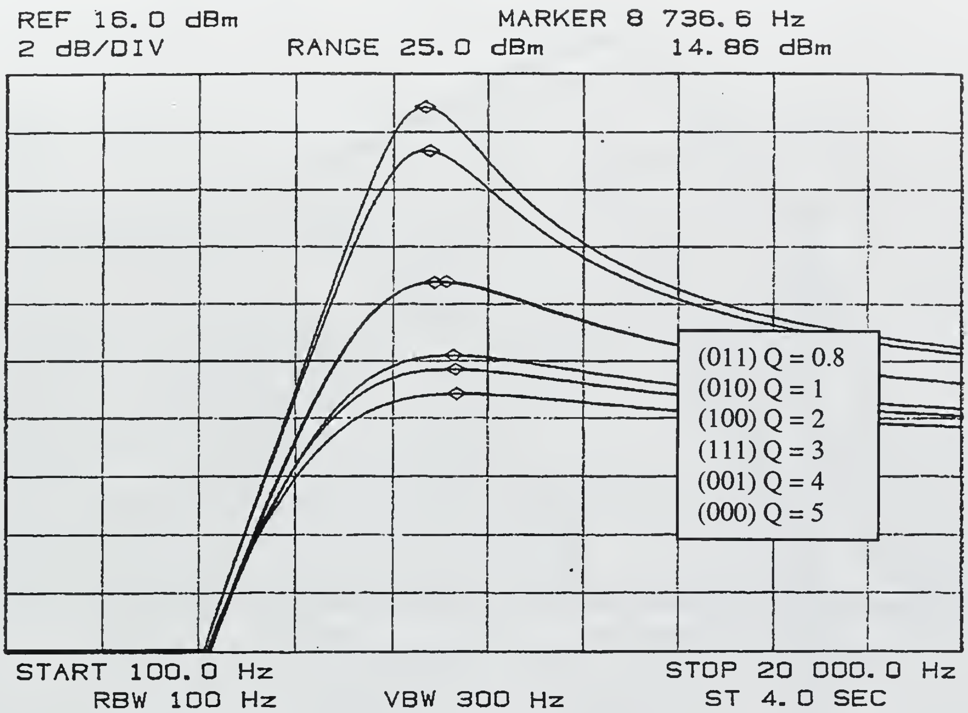



4. Notch Filter

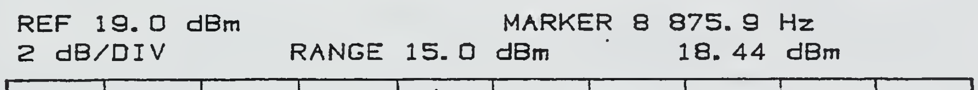


## C. GIC OUTPUT GRAPHS WITH Q = 0.8 - 5

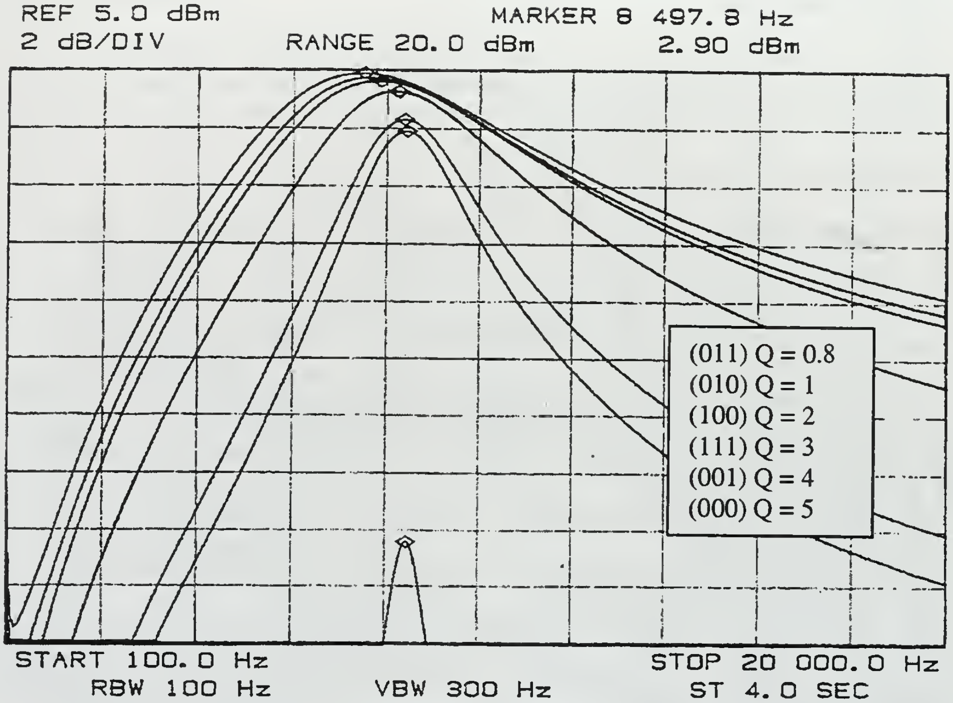
### 1. High Pass Filter



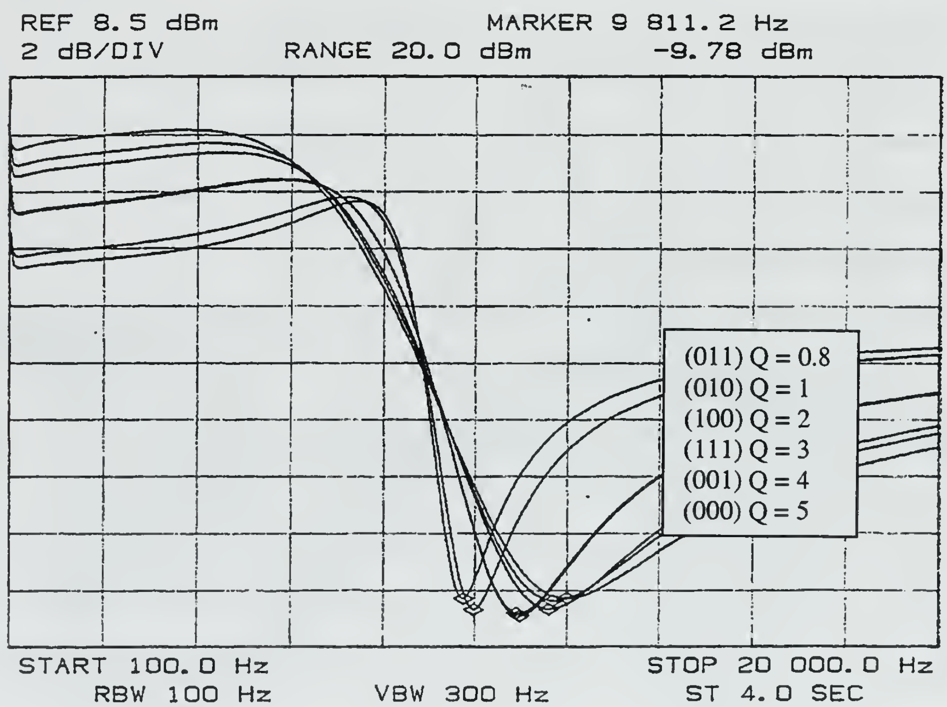

### 2. Low Pass Filter



### 3. Band Pass Filter




### 4. Notch Filter



National Semiconductor

February 1995

# LF411 Low Offset, Low Drift JFET Input Operational Amplifier

## General Description

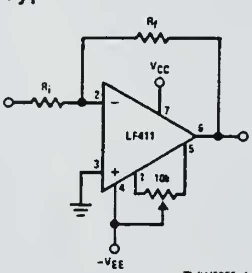
These devices are low cost, high speed, JFET input operational amplifiers with very low input offset voltage and guaranteed input offset voltage drift. They require low supply current yet maintain a large gain bandwidth product and fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents. The LF411 is pin compatible with the standard LM741 allowing designers to immediately upgrade the overall performance of existing designs.

These amplifiers may be used in applications such as high speed integrators, fast D/A converters, sample and hold circuits and many other circuits requiring low input offset voltage and drift, low input bias current, high input impedance, high slew rate and wide bandwidth.

## Features

- Internally trimmed offset voltage — 0.5 mV(max)
- Input offset voltage drift — 10 $\mu$V/°C(max)
- Low input bias current — 50 pA
- Low input noise current — 0.01 pA/$\sqrt{\text{Hz}}$
- Wide gain bandwidth — 3 MHz(min)
- High slew rate — 10V/$\mu$s(min)
- Low supply current — 1.8 mA
- High input impedance — $10^{12}\Omega$
- Low total harmonic distortion $A_V = 10$, $R_L = 10k$, $V_O = 20$ Vp-p, BW = 20 Hz−20 kHz — <0.02%
- Low 1/f noise corner — 50 Hz
- Fast settling time to 0.01% — 2 $\mu$s

## Typical Connection




TL/H/5655–1

## Ordering Information

LF411XYZ

X indicates electrical grade

Y indicates temperature range

"M" for military

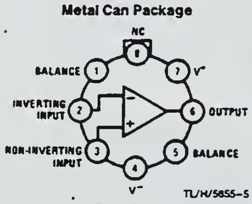
"C" for commercial

Z indicates package type

"H" or "N"

## Connection Diagrams

**Metal Can Package**




TL/H/5655–5

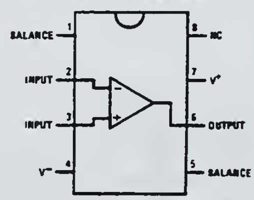
Top View

Note: Pin 4 connected to case.

Order Number LF411ACH or LF411MH/883*

See NS Package Number H08A

**Dual-In-Line Package**




TL/H/5655–7

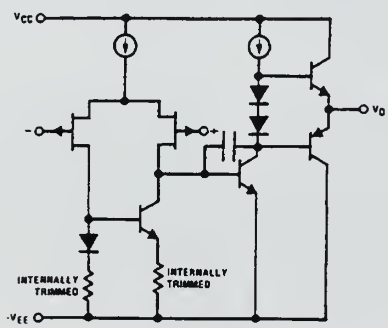
Top View

Order Number LF411ACN, LF411CN or LF411MJ/883*

See NS Package Number N08E or J08A

*Available per JM38510/11904

## Simplified Schematic




TL/H/5655–6

BI-FET II™ is a trademark of National Semiconductor Corporation.



RRD-B30M115/Printed in U. S. A.

## Absolute Maximum Ratings

**If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications. (Note 8)**

| | LF411A | LF411 |
|---|---|---|
| Supply Voltage | ±22V | ±18V |
| Differential Input Voltage | ±38V | ±30V |
| Input Voltage Range (Note 1) | ±19V | ±15V |
| Output Short Circuit Duration | Continuous | Continuous |

| | H Package | N Package |
|---|---|---|
| Power Dissipation (Notes 2 and 9) | 670 mW | 670 mW |
| $T_j$max | 150°C | 115°C |
| $\theta_jA$ | 162°C/W (Still Air) 65°C/W (400 LF/min Air Flow) | 120°C/W |
| $\theta_jC$ | 20°C/W | |
| Operating Temp. Range | (Note 3) | (Note 3) |
| Storage Temp. Range | $-65°C \le T_A \le 150°C$ | $-65°C \le T_A \le 150°C$ |
| Lead Temp. (Soldering, 10 sec.) | 260°C | 260°C |
| ESD Tolerance | | Rating to be determined. |

## DC Electrical Characteristics (Note 4)

| Symbol | Parameter | Conditions | | LF411A | | | LF411 | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | Min | Typ | Max | |
| $V_{OS}$ | Input Offset Voltage | $R_S = 10\,k\Omega$, $T_A = 25°C$ | | | 0.3 | 0.5 | | 0.8 | 2.0 | mV |
| $\Delta V_{OS}/\Delta T$ | Average TC of Input Offset Voltage | $R_S = 10\,k\Omega$ (Note 5) | | | 7 | 10 | | 7 | 20 (Note 5) | μV/°C |
| $I_{OS}$ | Input Offset Current | $V_S = \pm 15V$ (Notes 4, 6) | $T_j = 25°C$ | | 25 | 100 | | 25 | 100 | pA |
| | | | $T_j = 70°C$ | | | 2 | | | 2 | nA |
| | | | $T_j = 125°C$ | | | 25 | | | 25 | nA |
| $I_B$ | Input Bias Current | $V_S = \pm 15V$ (Notes 4, 6) | $T_j = 25°C$ | | 50 | 200 | | 50 | 200 | pA |
| | | | $T_j = 70°C$ | | | 4 | | | 4 | nA |
| | | | $T_j = 125°C$ | | | 50 | | | 50 | nA |
| $R_{IN}$ | Input Resistance | $T_j = 25°C$ | | | $10^{12}$ | | | $10^{12}$ | | Ω |
| $A_{VOL}$ | Large Signal Voltage Gain | $V_S = \pm 15V$ $V_O = \pm 10V$, $R_L = 2k$, $T_A = 25°C$ | | 50 | 200 | | 25 | 200 | | V/mV |
| | | Over Temperature | | 25 | 200 | | 15 | 200 | | V/mV |
| $V_O$ | Output Voltage Swing | $V_S = \pm 15V$, $R_L = 10k$ | | ±12 | ±13.5 | | ±12 | ±13.5 | | V |
| $V_{CM}$ | Input Common-Mode Voltage Range | | | ±16 | +19.5 | | ±11 | +14.5 | | V |
| | | | | | −16.5 | | | −11.5 | | V |
| CMRR | Common-Mode Rejection Ratio | $R_S \le 10k$ | | 80 | 100 | | 70 | 100 | | dB |
| PSRR | Supply Voltage Rejection Ratio | (Note 7) | | 80 | 100 | | 70 | 100 | | dB |
| $I_S$ | Supply Current | | | | 1.8 | 2.8 | | 1.8 | 3.4 | mA |

## AC Electrical Characteristics (Note 4)

| Symbol | Parameter | Conditions | LF411A | | | LF411 | | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Typ | Max | |
| SR | Slew Rate | $V_S = \pm 15V$, $T_A = 25°C$ | 10 | 15 | | 8 | 15 | | V/μs |
| GBW | Gain-Bandwidth Product | $V_S = \pm 15V$, $T_A = 25°C$ | 3 | 4 | | 2.7 | 4 | | MHz |
| $e_n$ | Equivalent Input Noise Voltage | $T_A = 25°C$, $R_S = 100\Omega$, f = 1 kHz | | 25 | | | 25 | | $nV/\sqrt{Hz}$ |
| $i_n$ | Equivalent Input Noise Current | $T_A = 25°C$, f = 1 kHz | | 0.01 | | | 0.01 | | $pA/\sqrt{Hz}$ |

**Note 1:** Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

**Note 2:** For operating at elevated temperature, these devices must be derated based on a thermal resistance of $\theta_{jA}$.

**Note 3:** These devices are available in both the commercial temperature range $0°C \leq T_A \leq 70°C$ and the military temperature range $-55°C \leq T_A \leq 125°C$. The temperature range is designated by the position just before the package type in the device number. A "C" indicates the commercial temperature range and an "M" indicates the military temperature range. The military temperature range is available in "H" package only.

**Note 4:** Unless otherwise specified, the specifications apply over the full temperature range and for $V_S = \pm 20V$ for the LF411A and for $V_S = \pm 15V$ for the LF411. $V_{OS}$, $I_B$, and $I_{OS}$ are measured at $V_{CM} = 0$.

**Note 5:** The LF411A is 100% tested to this specification. The LF411 is sample tested to insure at least 90% of the units meet this specification.

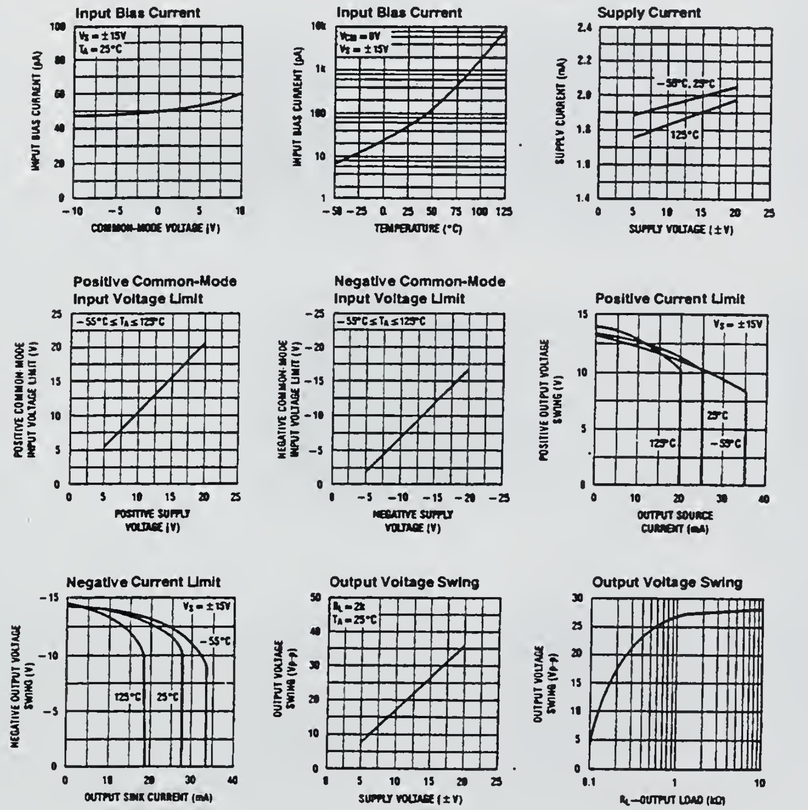
**Note 6:** The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, $T_j$. Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, $P_D$. $T_j = T_A + \theta_{jA} P_D$ where $\theta_{jA}$ is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

**Note 7:** Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously in accordance with common practice, from $\pm 15V$ to $\pm 5V$ for the LF411 and from $\pm 20V$ to $\pm 5V$ for the LF411A.

**Note 8:** RETS 411X for LF411MH and LF411MJ military specifications.

**Note 9:** Max. Power Dissipation is defined by the package characteristics. Operating the part near the Max. Power Dissipation may cause the part to operate outside guaranteed limits.

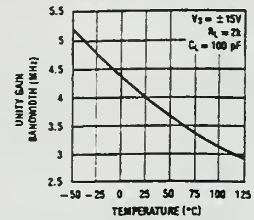
## Typical Performance Characteristics



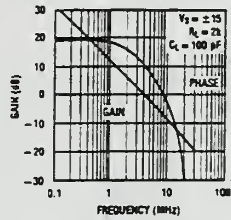

TL/H/5655-2

## Typical Performance Characteristics (Continued)

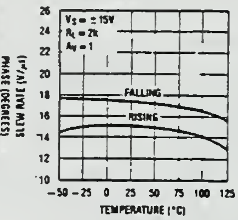
Gain Bandwidth



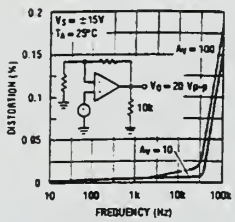

Bode Plot



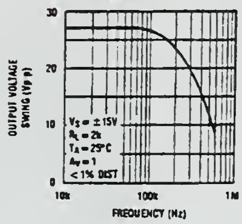

Slew Rate



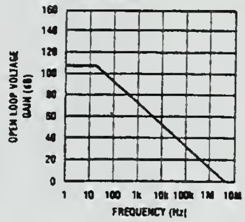

Distortion vs Frequency



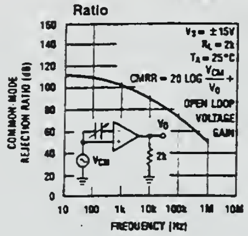

Undistorted Output Voltage Swing



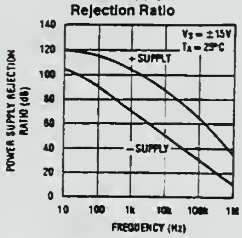

Open Loop Frequency Response



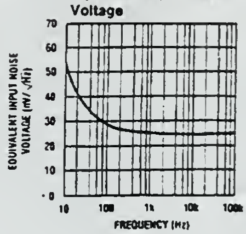

Common-Mode Rejection Ratio



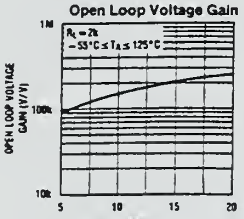

Power Supply Rejection Ratio



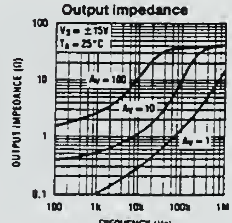

Equivalent Input Noise Voltage



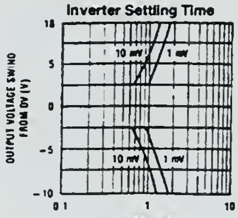

Open Loop Voltage Gain




Output Impedance



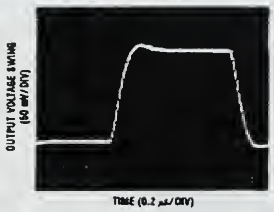

Inverter Settling Time



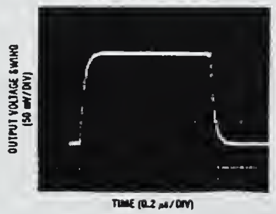

TL/H/5655–3

## Pulse Response $R_L = 2\ k\Omega$, $C_L$ 10 pF

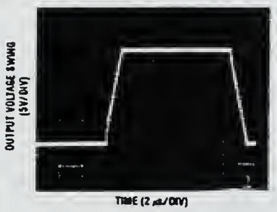
**Small Signal Inverting**



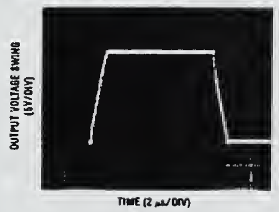

**Small Signal Non-Inverting**



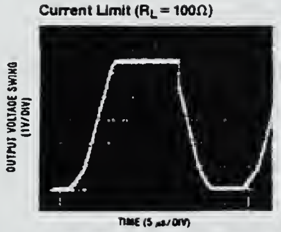

**Large Signal Inverting**




**Large Signal Non-Inverting**




**Current Limit ($R_L = 100\Omega$)**




TL/H/5655–4

## Application Hints

The LF411 series of internally trimmed JFET input op amps (BI-FET II™) provide very low input offset voltage and guaranteed input offset voltage drift. These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore, large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will force the output to a high state, potentially causing a reversal of phase to the output. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output; however, if both inputs exceed the limit, the output of the amplifier may be forced to a high state.

## Application Hints (Continued)

The amplifier will operate with a common-mode input voltage equal to the positive supply; however, the gain bandwidth and slew rate may be decreased in this condition. When the negative common-mode voltage swings to within 3V of the negative supply, an increase in input offset voltage may occur.

The LF411 is biased by a zener reference which allows normal circuit operation on ±4.5V power supplies. Supply voltages less than these may result in lower gain bandwidth and slew rate.

The LF411 will drive a 2 kΩ load resistance to ±10V over the full temperature range. If the amplifier is forced to drive heavier load currents, however, an increase in input offset voltage may occur on the negative voltage swing and finally reach an active current limit on both positive and negative swings.

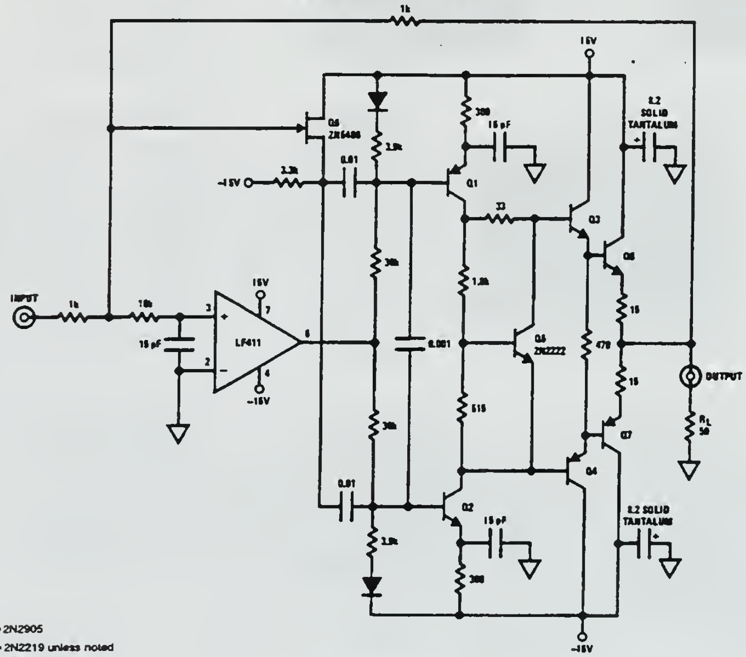
Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pick-up" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately 6 times the expected 3 dB frequency, a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

## Typical Applications

**High Speed Current Booster**




PNP = 2N2905
NPN = 2N2219 unless noted
TO-5 heat sinks for Q6-Q7

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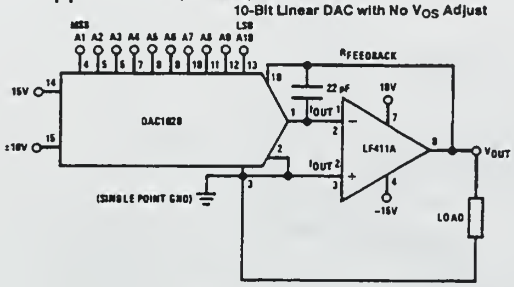
## Typical Applications (Continued)

**10-Bit Linear DAC with No $V_{OS}$ Adjust**




$$V_{OUT} = -V_{REF}\left(\frac{A1}{2} + \frac{A2}{4} + \frac{A3}{8} + \cdots \frac{A10}{1024}\right)$$

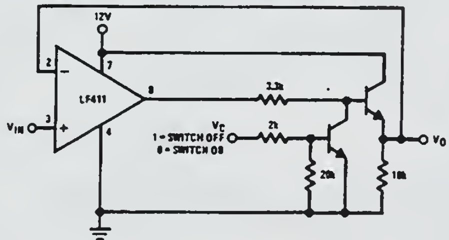
$-10V \leq V_{REF} \leq 10V$

$0 \leq V_{OUT} \leq -\frac{1023}{1024} V_{REF}$

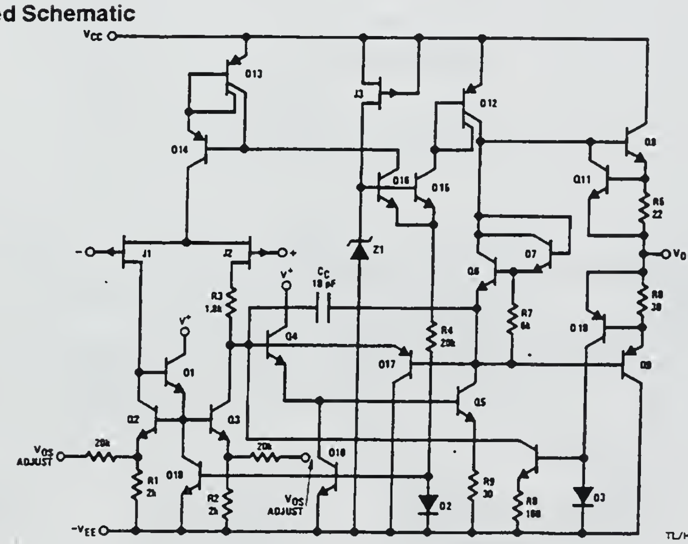
where $A_N = 1$ if the $A_N$ digital input is high

$A_N = 0$ if the $A_N$ digital input is low

**Single Supply Analog Switch with Buffered Output**




## Detailed Schematic




TL/H/5655-10

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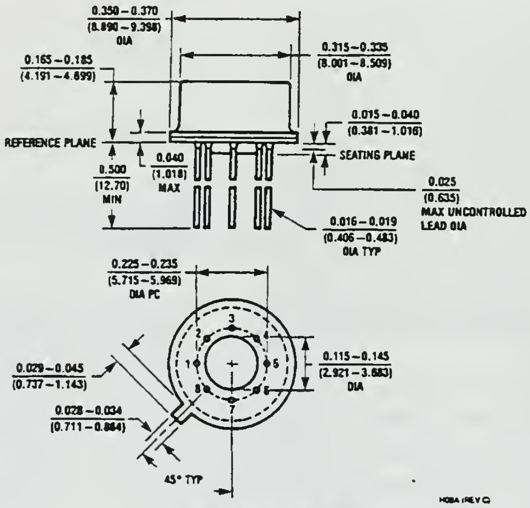
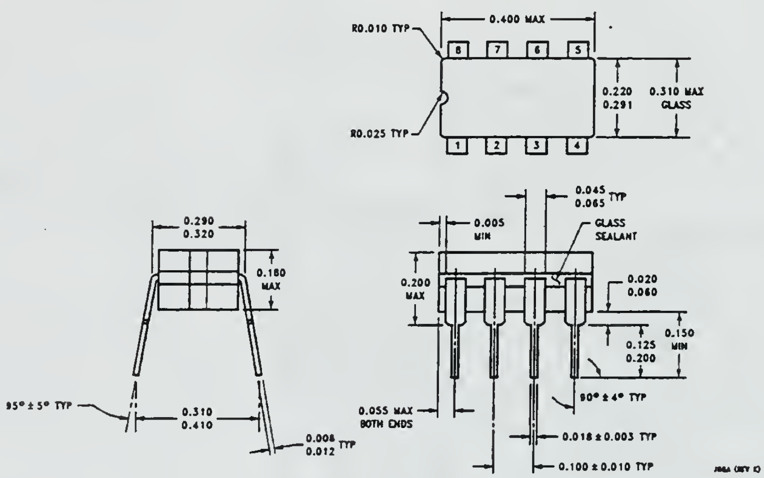
## Physical Dimensions inches (millimeters)




**Metal Can Package (H)**
**Order Number LF411MH/883 or LF411ACH**
**NS Package Number H08A**




**Ceramic Dual-In-Line Package (J)**
**Order Number LF411MJ/883**
**NS Package Number J08A**

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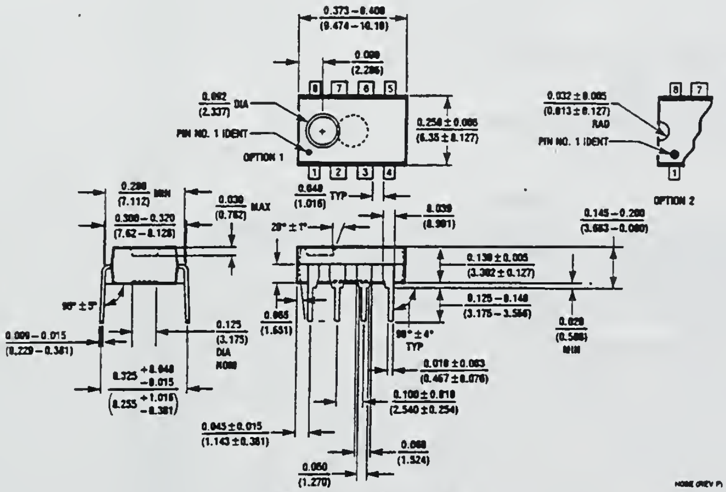
## Physical Dimensions inches (millimeters) (Continued)




**Molded Dual-In-Line Package (N)**
**Order Number LF411ACN or LF411CN**
**NS Package Number N08E**

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National Semiconductor

March 1988

# CD4001BM/CD4001BC Quad 2-Input NOR Buffered B Series Gate CD4011BM/CD4011BC Quad 2-Input NAND Buffered B Series Gate

## General Description

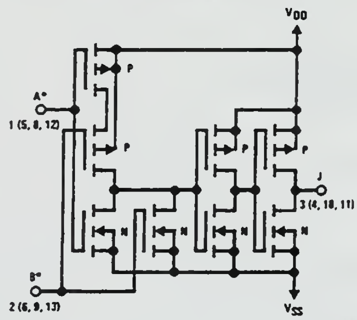
These quad gates are monolithic complementary MOS (CMOS) integrated circuits constructed with N- and P-channel enhancement mode transistors. They have equal source and sink current capabilities and conform to standard B series output drive. The devices also have buffered outputs which improve transfer characteristics by providing very high gain.

All inputs are protected against static discharge with diodes to $V_{DD}$ and $V_{SS}$.

## Features

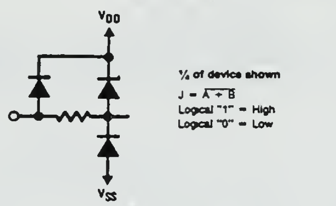
- Low power TTL compatibility — Fan out of 2 driving 74L or 1 driving 74LS
- 5V–10V–15V parametric ratings
- Symmetrical output characteristics
- Maximum input leakage 1 µA at 15V over full temperature range

## Schematic Diagrams



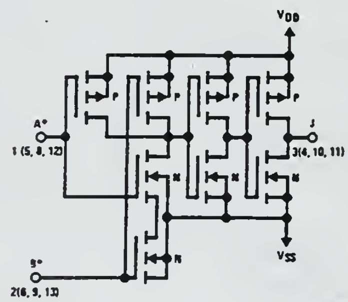

TL/F/5939-1

CD4001BC/BM



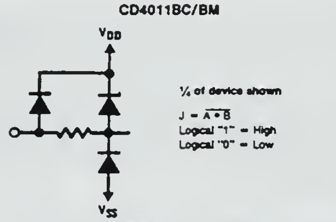

TL/F/5939-2

*All inputs protected by standard CMOS protection circuit.




TL/F/5939-5

CD4011BC/BM




TL/F/5939-6

*All inputs protected by standard CMOS protection circuit.

 RRD-B30M105/Printed in U. S. A.

## Absolute Maximum Ratings (Notes 1 and 2)

**If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.**

| | |
|---|---|
| Voltage at any Pin | $-0.5V$ to $V_{DD}$ $+0.5V$ |
| Power Dissipation ($P_D$) | |
| Dual-In-Line | 700 mW |
| Small Outline | 500 mW |
| $V_{DD}$ Range | $-0.5\ V_{DC}$ to $+18\ V_{DC}$ |
| Storage Temperature ($T_S$) | $-65°C$ to $+150°C$ |
| Lead Temperature ($T_L$) (Soldering, 10 seconds) | 260°C |

## Operating Conditions

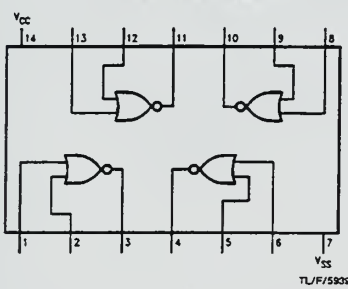
| | |
|---|---|
| Operating Range ($V_{DD}$) | $3\ V_{DC}$ to $15\ V_{DC}$ |
| Operating Temperature Range | |
| CD4001BM, CD4011BM | $-55°C$ to $+125°C$ |
| CD4001BC, CD4011BC | $-40°C$ to $+85°C$ |

## DC Electrical Characteristics CD4001BM, CD4011BM (Note 2)

| Symbol | Parameter | Conditions | −55°C | | +25°C | | | +125°C | | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Typ | Max | Min | Max | |
| $I_{DD}$ | Quiescent Device Current | $V_{DD}=5V$, $V_{IN}=V_{DD}$ or $V_{SS}$ | | 0.25 | | 0.004 | 0.25 | | 7.5 | μA |
| | | $V_{DD}=10V$, $V_{IN}=V_{DD}$ or $V_{SS}$ | | 0.50 | | 0.005 | 0.50 | | 15 | μA |
| | | $V_{DD}=15V$, $V_{IN}=V_{DD}$ or $V_{SS}$ | | 1.0 | | 0.006 | 1.0 | | 30 | μA |
| $V_{OL}$ | Low Level Output Voltage | $V_{DD}=5V$, $\|I_O\|<1\ \mu A$ | | 0.05 | | 0 | 0.05 | | 0.05 | V |
| | | $V_{DD}=10V$, $\|I_O\|<1\ \mu A$ | | 0.05 | | 0 | 0.05 | | 0.05 | V |
| | | $V_{DD}=15V$, $\|I_O\|<1\ \mu A$ | | 0.05 | | 0 | 0.05 | | 0.05 | V |
| $V_{OH}$ | High Level Output Voltage | $V_{DD}=5V$, $\|I_O\|<1\ \mu A$ | 4.95 | | 4.95 | 5 | | 4.95 | | V |
| | | $V_{DD}=10V$, $\|I_O\|<1\ \mu A$ | 9.95 | | 9.95 | 10 | | 9.95 | | V |
| | | $V_{DD}=15V$, $\|I_O\|<1\ \mu A$ | 14.95 | | 14.95 | 15 | | 14.95 | | V |
| $V_{IL}$ | Low Level Input Voltage | $V_{DD}=5V$, $V_O=4.5V$ | | 1.5 | | 2 | 1.5 | | 1.5 | V |
| | | $V_{DD}=10V$, $V_O=9.0V$ | | 3.0 | | 4 | 3.0 | | 3.0 | V |
| | | $V_{DD}=15V$, $V_O=13.5V$ | | 4.0 | | 6 | 4.0 | | 4.0 | V |
| $V_{IH}$ | High Level Input Voltage | $V_{DD}=5V$, $V_O=0.5V$ | 3.5 | | 3.5 | 3 | | 3.5 | | V |
| | | $V_{DD}=10V$, $V_O=1.0V$ | 7.0 | | 7.0 | 6 | | 7.0 | | V |
| | | $V_{DD}=15V$, $V_O=1.5V$ | 11.0 | | 11.0 | 9 | | 11.0 | | V |
| $I_{OL}$ | Low Level Output Current (Note 3) | $V_{DD}=5V$, $V_O=0.4V$ | 0.64 | | 0.51 | 0.88 | | 0.36 | | mA |
| | | $V_{DD}=10V$, $V_O=0.5V$ | 1.6 | | 1.3 | 2.25 | | 0.9 | | mA |
| | | $V_{DD}=15V$, $V_O=1.5V$ | 4.2 | | 3.4 | 8.8 | | 2.4 | | mA |
| $I_{OH}$ | High Level Output Current (Note 3) | $V_{DD}=5V$, $V_O=4.6V$ | −0.64 | | −0.51 | −0.88 | | −0.36 | | mA |
| | | $V_{DD}=10V$, $V_O=9.5V$ | −1.6 | | −1.3 | −2.25 | | −0.9 | | mA |
| | | $V_{DD}=15V$, $V_O=13.5V$ | −4.2 | | −3.4 | −8.8 | | −2.4 | | mA |
| $I_{IN}$ | Input Current | $V_{DD}=15V$, $V_{IN}=0V$ | | −0.10 | | $-10^{-5}$ | −0.10 | | −1.0 | μA |
| | | $V_{DD}=15V$, $V_{IN}=15V$ | | 0.10 | | $10^{-5}$ | 0.10 | | 1.0 | μA |

## Connection Diagrams

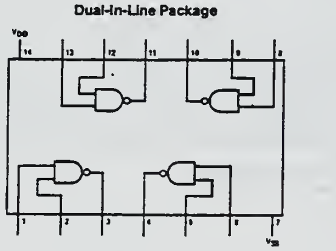
**CD4001BC/CD4001BM**
**Dual-In-Line Package**




TL/F/5939-3

Top View

**CD4011BC/CD4011BM**
**Dual-In-Line Package**



TL/F/5939-4

**Top View**

**Order Number CD4001B or CD4011B**

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## DC Electrical Characteristics CD4001BC, CD4011BC (Note 2)

| Symbol | Parameter | Conditions | −40°C Min | −40°C Max | +25°C Min | +25°C Typ | +25°C Max | +85°C Min | +85°C Max | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| $I_{DD}$ | Quiescent Device Current | $V_{DD}$ = 5V, $V_{IN}$ = $V_{DD}$ or $V_{SS}$ | | 1 | | 0.004 | 1 | | 7.5 | μA |
| | | $V_{DD}$ = 10V, $V_{IN}$ = $V_{DD}$ or $V_{SS}$ | | 2 | | 0.005 | 2 | | 15 | μA |
| | | $V_{DD}$ = 15V, $V_{IN}$ = $V_{DD}$ or $V_{SS}$ | | 4 | | 0.006 | 4 | | 30 | μA |
| $V_{OL}$ | Low Level Output Voltage | $V_{DD}$ = 5V, $\lvert I_O \rvert$ < 1 μA | | 0.05 | | 0 | 0.05 | | 0.05 | V |
| | | $V_{DD}$ = 10V, $\lvert I_O \rvert$ < 1 μA | | 0.05 | | 0 | 0.05 | | 0.05 | V |
| | | $V_{DD}$ = 15V, $\lvert I_O \rvert$ < 1 μA | | 0.05 | | 0 | 0.05 | | 0.05 | V |
| $V_{OH}$ | High Level Output Voltage | $V_{DD}$ = 5V, $\lvert I_O \rvert$ < 1 μA | 4.95 | | 4.95 | 5 | | 4.95 | | V |
| | | $V_{DD}$ = 10V, $\lvert I_O \rvert$ < 1 μA | 9.95 | | 9.95 | 10 | | 9.95 | | V |
| | | $V_{DD}$ = 15V, $\lvert I_O \rvert$ < 1 μA | 14.95 | | 14.95 | 15 | | 14.95 | | V |
| $V_{IL}$ | Low Level Input Voltage | $V_{DD}$ = 5V, $V_O$ = 4.5V | | 1.5 | | 2 | 1.5 | | 1.5 | V |
| | | $V_{DD}$ = 10V, $V_O$ = 9.0V | | 3.0 | | 4 | 3.0 | | 3.0 | V |
| | | $V_{DD}$ = 15V, $V_O$ = 13.5V | | 4.0 | | 6 | 4.0 | | 4.0 | V |
| $V_{IH}$ | High Level Input Voltage | $V_{DD}$ = 5V, $V_O$ = 0.5V | 3.5 | | 3.5 | 3 | | 3.5 | | V |
| | | $V_{DD}$ = 10V, $V_O$ = 1.0V | 7.0 | | 7.0 | 6 | | 7.0 | | V |
| | | $V_{DD}$ = 15V, $V_O$ = 1.5V | 11.0 | | 11.0 | 9 | | 11.0 | | V |
| $I_{OL}$ | Low Level Output Current (Note 3) | $V_{DD}$ = 5V, $V_O$ = 0.4V | 0.52 | | 0.44 | 0.88 | | 0.36 | | mA |
| | | $V_{DD}$ = 10V, $V_O$ = 0.5V | 1.3 | | 1.1 | 2.25 | | 0.9 | | mA |
| | | $V_{DD}$ = 15V, $V_O$ = 1.5V | 3.6 | | 3.0 | 8.8 | | 2.4 | | mA |
| $I_{OH}$ | High Level Output Current (Note 3) | $V_{DD}$ = 5V, $V_O$ = 4.6V | −0.52 | | −0.44 | −0.88 | | −0.36 | | mA |
| | | $V_{DD}$ = 10V, $V_O$ = 9.5V | −1.3 | | −1.1 | −2.25 | | −0.9 | | mA |
| | | $V_{DD}$ = 15V, $V_O$ = 13.5V | −3.6 | | −3.0 | −8.8 | | −2.4 | | mA |
| $I_{IN}$ | Input Current | $V_{DD}$ = 15V, $V_{IN}$ = 0V | | −0.30 | | $-10^{-5}$ | −0.30 | | −1.0 | μA |
| | | $V_{DD}$ = 15V, $V_{IN}$ = 15V | | 0.30 | | $10^{-5}$ | 0.30 | | 1.0 | μA |

## AC Electrical Characteristics* CD4001BC, CD4001BM

$T_A$ = 25°C, Input $t_r$; $t_f$ = 20 ns. $C_L$ = 50 pF, $R_L$ = 200k. Typical temperature coefficient is 0.3%/°C.

| Symbol | Parameter | Conditions | Typ | Max | Units |
|---|---|---|---|---|---|
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level | $V_{DD}$ = 5V | 120 | 250 | ns |
| | | $V_{DD}$ = 10V | 50 | 100 | ns |
| | | $V_{DD}$ = 15V | 35 | 70 | ns |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level | $V_{DD}$ = 5V | 110 | 250 | ns |
| | | $V_{DD}$ = 10V | 50 | 100 | ns |
| | | $V_{DD}$ = 15V | 35 | 70 | ns |
| $t_{THL}$, $t_{TLH}$ | Transition Time | $V_{DD}$ = 5V | 90 | 200 | ns |
| | | $V_{DD}$ = 10V | 50 | 100 | ns |
| | | $V_{DD}$ = 15V | 40 | 80 | ns |
| $C_{IN}$ | Average Input Capacitance | Any Input | 5 | 7.5 | pF |
| $C_{PD}$ | Power Dissipation Capacity | Any Gate | 14 | | pF |

*AC Parameters are guaranteed by DC correlated testing.

**Note 1:** "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

**Note 2:** All voltages measured with respect to $V_{SS}$ unless otherwise specified.

**Note 3:** $I_{OL}$ and $I_{OH}$ are tested one output at a time.

## AC Electrical Characteristics* CD4011BC, CD4011BM

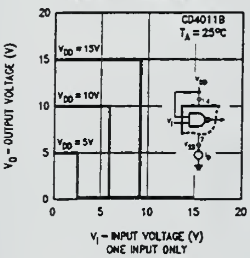
$T_A = 25°C$, Input $t_r$; $t_f$ = 20 ns. $C_L$ = 50 pF, $R_L$ = 200k. Typical Temperature Coefficient is 0.3%/°C.

| Symbol | Parameter | Conditions | Typ | Max | Units |
|---|---|---|---|---|---|
| $t_{PHL}$ | Propagation Delay, High-to-Low Level | $V_{DD}$ = 5V | 120 | 250 | ns |
| | | $V_{DD}$ = 10V | 50 | 100 | ns |
| | | $V_{DD}$ = 15V | 35 | 70 | ns |
| $t_{PLH}$ | Propagation Delay, Low-to-High Level | $V_{DD}$ = 5V | 85 | 250 | ns |
| | | $V_{DD}$ = 10V | 40 | 100 | ns |
| | | $V_{DD}$ = 15V | 30 | 70 | ns |
| $t_{THL}$, $t_{TLH}$ | Transition Time | $V_{DD}$ = 5V | 90 | 200 | ns |
| | | $V_{DD}$ = 10V | 50 | 100 | ns |
| | | $V_{DD}$ = 15V | 40 | 80 | ns |
| $C_{IN}$ | Average Input Capacitance | Any Input | 5 | 7.5 | pF |
| $C_{PD}$ | Power Dissipation Capacity | Any Gate | 14 | | pF |

*AC Parameters are guaranteed by DC correlated testing.

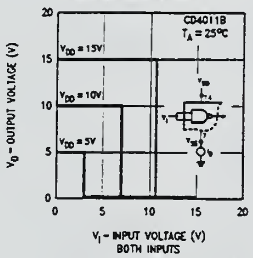
## Typical Performance Characteristics

**Typical Transfer Characteristics**



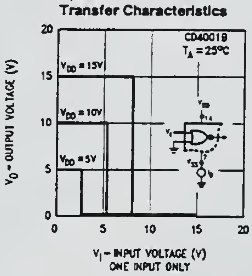

TL/F/5939–7

**Typical Transfer Characteristics**



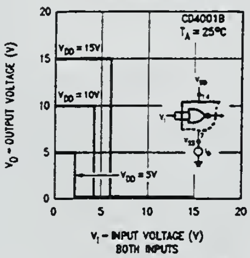

TL/F/5939–8

**Typical Transfer Characteristics**

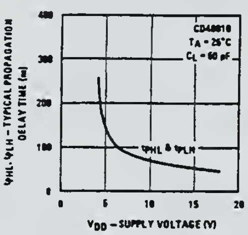



TL/F/5939–9

**Typical Transfer Characteristics**

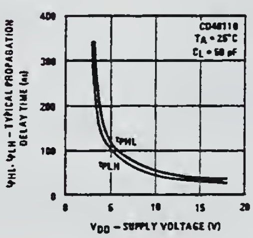



TL/F/5939–10




TL/F/5939–11

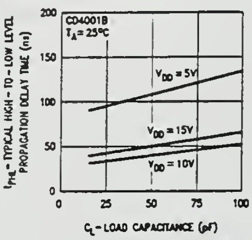
FIGURE 5




TL/F/5939–12

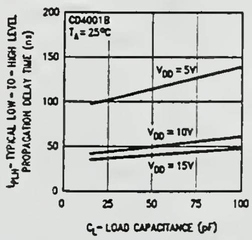
FIGURE 6

## Typical Performance Characteristics (Continued)



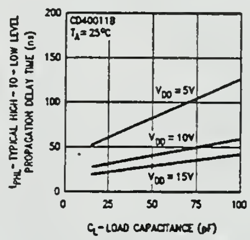
TL/F/5939–13

FIGURE 7



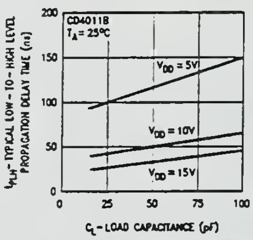
TL/F/5939–14

FIGURE 8



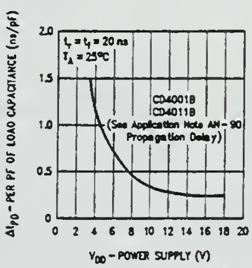
TL/F/5939–15

FIGURE 9



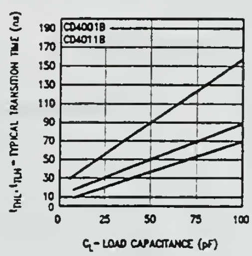
TL/F/5939–16

FIGURE 10



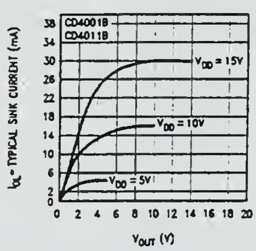
TL/F/5939–17

FIGURE 11



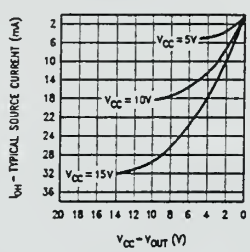
TL/F/5939–18

FIGURE 12



TL/F/5939–19

FIGURE 13

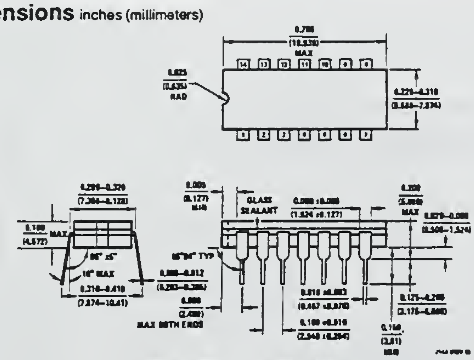


TL/F/5939–20

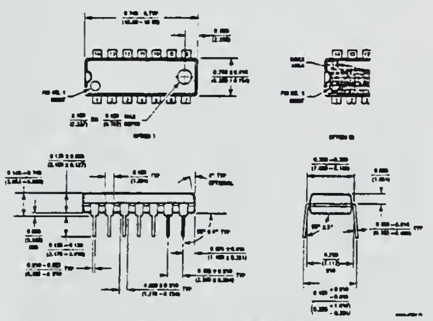
FIGURE 14

5

## Physical Dimensions inches (millimeters)



**Ceramic Dual-In-Line Package (J)**
**Order Number CD4001BMJ, CD4001BCJ, CD40011BMJ or CD4011BCJ**
**NS Package Number J14A**



**Molded Dual-In-Line Package (N)**
**Order Number CD4001BMN, CD4001BCN, CD4011BMN or CD4011BCN**
**NS Package Number N14A**



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Fax: 81-043-299-2408

National Semiconductor

March 1988

# CD4049UBM/CD4049UBC Hex Inverting Buffer
# CD4050BM/CD4050BC Hex Non-Inverting Buffer

## General Description

These hex buffers are monolithic complementary MOS (CMOS) integrated circuits constructed with N- and P-channel enhancement mode transistors. These devices feature logic level conversion using only one supply voltage ($V_{DD}$). The input signal high level ($V_{IH}$) can exceed the $V_{DD}$ supply voltage when these devices are used for logic level conversions. These devices are intended for use as hex buffers, CMOS to DTL/TTL converters, or as CMOS current drivers, and at $V_{DD}$ = 5.0V, they can drive directly two DTL/TTL loads over the full operating temperature range.

## Features

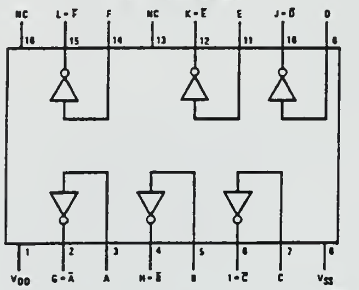
- Wide supply voltage range 3.0V to 15V
- Direct drive to 2 TTL loads at 5.0V over full temperature range
- High source and sink current capability
- Special input protection permits input voltages greater than $V_{DD}$

## Applications

- CMOS hex inverter/buffer
- CMOS to DTL/TTL hex converter
- CMOS current "sink" or "source" driver
- CMOS high-to-low logic level converter

## Connection Diagrams

**CD4049UBM/CD4049UBC**
**Dual-In-Line Package**

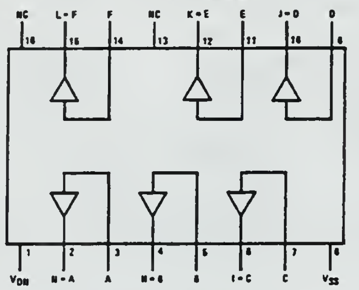


TL/F/5971-1

**Top View**

**Order Number CD4049UB or CD4049B**

**CD4050BM/CD4050BC**
**Dual-In-Line Package**



TL/F/5971-2

**Top View**

**Order Number CD4050UB or CD4050B**



RRD-B30M105/Printed in U. S. A.

## Absolute Maximum Ratings (Notes 1 & 2)

**If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.**

| | |
|---|---|
| Supply Voltage ($V_{DD}$) | −0.5V to +18V |
| Input Voltage ($V_{IN}$) | −0.5V to +18V |
| Voltage at Any Output Pin ($V_{OUT}$) | −0.5V to $V_{DD}$ + 0.5V |
| Storage Temperature Range ($T_S$) | −65°C to +150°C |
| Power Dissipation ($P_D$) | |
| Dual-In-Line | 700 mW |
| Small Outline | 500 mW |
| Lead Temperature ($T_L$) (Soldering, 10 seconds) | 260°C |

## Recommended Operating Conditions (Note 2)

| | |
|---|---|
| Supply Voltage ($V_{DD}$) | 3V to 15V |
| Input Voltage ($V_{IN}$) | 0V to 15V |
| Voltage at Any Output Pin ($V_{OUT}$) | 0 to $V_{DD}$ |
| Operating Temperature Range ($T_A$) | |
| CD4049UBM, CD4050BM | −55°C to +125°C |
| CD4049UBC, CD4050BC | −40°C to +85°C |

## DC Electrical Characteristics CD4049M/CD4050BM (Note 2)

| Symbol | Parameter | Conditions | −55°C | | +25°C | | | +125°C | | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Typ | Max | Min | Max | |
| $I_{DD}$ | Quiescent Device Current | $V_{DD}$ = 5V | | 1.0 | | 0.01 | 1.0 | | 30 | μA |
| | | $V_{DD}$ = 10V | | 2.0 | | 0.01 | 2.0 | | 60 | μA |
| | | $V_{DD}$ = 15V | | 4.0 | | 0.03 | 4.0 | | 120 | μA |
| $V_{OL}$ | Low Level Output Voltage | $V_{IH}$ = $V_{DD}$, $V_{IL}$ = 0V, $\lvert I_O \rvert$ < 1 μA | | | | | | | | |
| | | $V_{DD}$ = 5V | | 0.05 | | 0 | 0.05 | | 0.05 | V |
| | | $V_{DD}$ = 10V | | 0.05 | | 0 | 0.05 | | 0.05 | V |
| | | $V_{DD}$ = 15V | | 0.05 | | 0 | 0.05 | | 0.05 | V |
| $V_{OH}$ | High Level Output Voltage | $V_{IH}$ = $V_{DD}$, $V_{IL}$ = 0V, $\lvert I_O \rvert$ < 1 μA | | | | | | | | |
| | | $V_{DD}$ = 5V | 4.95 | | 4.95 | 5 | | 4.95 | | V |
| | | $V_{DD}$ = 10V | 9.95 | | 9.95 | 10 | | 9.95 | | V |
| | | $V_{DD}$ = 15V | 14.95 | | 14.95 | 15 | | 14.95 | | V |
| $V_{IL}$ | Low Level Input Voltage (CD4050BM Only) | $\lvert I_O \rvert$ < 1 μA | | | | | | | | |
| | | $V_{DD}$ = 5V, $V_O$ = 0.5V | | 1.5 | | 2.25 | 1.5 | | 1.5 | V |
| | | $V_{DD}$ = 10V, $V_O$ = 1V | | 3.0 | | 4.5 | 3.0 | | 3.0 | V |
| | | $V_{DD}$ = 15V, $V_O$ = 1.5V | | 4.0 | | 6.75 | 4.0 | | 4.0 | V |
| $V_{IL}$ | Low Level Input Voltage (CD4049UBM Only) | $\lvert I_O \rvert$ < 1 μA | | | | | | | | |
| | | $V_{DD}$ = 5V, $V_O$ = 4.5V | | 1.0 | | 1.5 | 1.0 | | 1.0 | V |
| | | $V_{DD}$ = 10V, $V_O$ = 9V | | 2.0 | | 2.5 | 2.0 | | 2.0 | V |
| | | $V_{DD}$ = 15V, $V_O$ = 13.5V | | 3.0 | | 3.5 | 3.0 | | 3.0 | V |
| $V_{IH}$ | High Level Input Voltage (CD4050BM Only) | $\lvert I_O \rvert$ < 1 μA | | | | | | | | |
| | | $V_{DD}$ = 5V, $V_O$ = 4.5V | 3.5 | | 3.5 | 2.75 | | 3.5 | | V |
| | | $V_{DD}$ = 10V, $V_O$ = 9V | 7.0 | | 7.0 | 5.5 | | 7.0 | | V |
| | | $V_{DD}$ = 15V, $V_O$ = 13.5V | 11.0 | | 11.0 | 8.25 | | 11.0 | | V |
| $V_{IH}$ | High Level Input Voltage (CD4049UBM Only) | $\lvert I_O \rvert$ < 1 μA | | | | | | | | |
| | | $V_{DD}$ = 5V, $V_O$ = 0.5V | 4.0 | | 4.0 | 3.5 | | 4.0 | | V |
| | | $V_{DD}$ = 10V, $V_O$ = 1V | 8.0 | | 8.0 | 7.5 | | 8.0 | | V |
| | | $V_{DD}$ = 15V, $V_O$ = 1.5V | 12.0 | | 12.0 | 11.5 | | 12.0 | | V |
| $I_{OL}$ | Low Level Output Current (Note 3) | $V_{IH}$ = $V_{DD}$, $V_{IL}$ = 0V | | | | | | | | |
| | | $V_{DD}$ = 5V, $V_O$ = 0.4V | 5.6 | | 4.6 | 5 | | 3.2 | | mA |
| | | $V_{DD}$ = 10V, $V_O$ = 0.5V | 12 | | 9.8 | 12 | | 6.8 | | mA |
| | | $V_{DD}$ = 15V, $V_O$ = 1.5V | 35 | | 29 | 40 | | 20 | | mA |

**Note 1:** "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed; they are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

**Note 2:** $V_{SS}$ = 0V unless otherwise specified.

**Note 3:** These are *peak* output current capabilities. Continuous output current is rated at 12 mA maximum. The output current should not be allowed to exceed this value for extended periods of time. $I_{OL}$ and $I_{OH}$ are tested one output at a time.

## DC Electrical Characteristics CD4049M/CD4050BM (Note 2) (Continued)

| Symbol | Parameter | Conditions | −55°C | | +25°C | | | +125°C | | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Typ | Max | Min | Max | |
| $I_{OH}$ | High Level Output Current (Note 3) | $V_{IH} = V_{DD}, V_{IL} = 0V$ | | | | | | | | |
| | | $V_{DD} = 5V, V_O = 4.6V$ | −1.3 | | −1.1 | −1.6 | | −0.72 | | mA |
| | | $V_{DD} = 10V, V_O = 9.5V$ | −2.6 | | −2.2 | −3.6 | | −1.5 | | mA |
| | | $V_{DD} = 15V, V_O = 13.5V$ | −8.0 | | −7.2 | −12 | | −5.0 | | mA |
| $I_{IN}$ | Input Current | $V_{DD} = 15V, V_{IN} = 0V$ | | −0.1 | | $-10^{-5}$ | −0.1 | | −1.0 | μA |
| | | $V_{DD} = 15V, V_{IN} = 15V$ | | 0.1 | | $10^{-5}$ | 0.1 | | 1.0 | μA |

**Note 1:** "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed; they are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

**Note 2:** $V_{SS}$ = 0V unless otherwise specified.

**Note 3:** These are *peak* output current capabilities. Continuous output current is rated at 12 mA maximum. The output current should not be allowed to exceed this value for extended periods of time. $I_{OL}$ and $I_{OH}$ are tested one output at a time.

## DC Electrical Characteristics CD4049UBC/CD4050BC (Note 2)

| Symbol | Parameter | Conditions | −40°C | | +25°C | | | +85°C | | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Typ | Max | Min | Max | |
| $I_{DD}$ | Quiescent Device Current | $V_{DD} = 5V$ | | 4 | | 0.03 | 4.0 | | 30 | μA |
| | | $V_{DD} = 10V$ | | 8 | | 0.05 | 8.0 | | 60 | μA |
| | | $V_{DD} = 15V$ | | 16 | | 0.07 | 16.0 | | 120 | μA |
| $V_{OL}$ | Low Level Output Voltage | $V_{IH} = V_{DD}, V_{IL} = 0V,$ | | | | | | | | |
| | | $\lvert I_O \rvert < 1\ \mu A$ | | | | | | | | |
| | | $V_{DD} = 5V$ | | 0.05 | | 0 | 0.05 | | 0.05 | V |
| | | $V_{DD} = 10V$ | | 0.05 | | 0 | 0.05 | | 0.05 | V |
| | | $V_{DD} = 15V$ | | 0.05 | | 0 | 0.05 | | 0.05 | V |
| $V_{OH}$ | High Level Output Voltage | $V_{IH} = V_{DD}, V_{IL} = 0V,$ | | | | | | | | |
| | | $\lvert I_O \rvert < 1\ \mu A$ | | | | | | | | |
| | | $V_{DD} = 5V$ | 4.95 | | 4.95 | 5 | | 4.95 | | V |
| | | $V_{DD} = 10V$ | 9.95 | | 9.95 | 10 | | 9.95 | | V |
| | | $V_{DD} = 15V$ | 14.95 | | 14.95 | 15 | | 14.95 | | V |
| $V_{IL}$ | Low Level Input Voltage (CD4050BC Only) | $\lvert I_O \rvert < 1\ \mu A$ | | | | | | | | |
| | | $V_{DD} = 5V, V_O = 0.5V$ | | 1.5 | | 2.25 | 1.5 | | 1.5 | V |
| | | $V_{DD} = 10V, V_O = 1V$ | | 3.0 | | 4.5 | 3.0 | | 3.0 | V |
| | | $V_{DD} = 15V, V_O = 1.5V$ | | 4.0 | | 6.75 | 4.0 | | 4.0 | V |
| $V_{IL}$ | Low Level Input Voltage (CD4049UBC Only) | $\lvert I_O \rvert < 1\ \mu A$ | | | | | | | | |
| | | $V_{DD} = 5V, V_O = 4.5V$ | | 1.0 | | 1.5 | 1.0 | | 1.0 | V |
| | | $V_{DD} = 10V, V_O = 9V$ | | 2.0 | | 2.5 | 2.0 | | 2.0 | V |
| | | $V_{DD} = 15V, V_O = 13.5V$ | | 3.0 | | 3.5 | 3.0 | | 3.0 | V |
| $V_{IH}$ | High Level Input Voltage (CD4050BC Only) | $\lvert I_O \rvert < 1\ \mu A$ | | | | | | | | |
| | | $V_{DD} = 5V, V_O = 4.5V$ | 3.5 | | 3.5 | 2.75 | | 3.5 | | V |
| | | $V_{DD} = 10V, V_O = 9V$ | 7.0 | | 7.0 | 5.5 | | 7.0 | | V |
| | | $V_{DD} = 15V, V_O = 13.5V$ | 11.0 | | 11.0 | 8.25 | | 11.0 | | V |
| $V_{IH}$ | High Level Input Voltage (CD4049UBC Only) | $\lvert I_O \rvert < 1\ \mu A$ | | | | | | | | |
| | | $V_{DD} = 5V, V_O = 0.5V$ | 4.0 | | 4.0 | 3.5 | | 4.0 | | V |
| | | $V_{DD} = 10V, V_O = 1V$ | 8.0 | | 8.0 | 7.5 | | 8.0 | | V |
| | | $V_{DD} = 15V, V_O = 1.5V$ | 12.0 | | 12.0 | 11.5 | | 12.0 | | V |

**Note 1:** "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed; they are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

**Note 2:** $V_{SS}$ = 0V unless otherwise specified.

**Note 3:** These are *peak* output current capabilities. Continuous output current is rated at 12 mA maximum. The output current should not be allowed to exceed this value for extended periods of time. $I_{OL}$ and $I_{OH}$ are tested one output at a time.

## DC Electrical Characteristics CD4049UBC/CD4050BC (Note 2) (Continued)

| Symbol | Parameter | Conditions | −40°C | | +25°C | | | +85°C | | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Typ | Max | Min | Max | |
| $I_{OL}$ | Low Level Output Current (Note 3) | $V_{IH} = V_{DD}$, $V_{IL} = 0V$ | | | | | | | | |
| | | $V_{DD} = 5V$, $V_D = 0.4V$ | 4.6 | | 4.0 | 5 | | 3.2 | | mA |
| | | $V_{DD} = 10V$, $V_O = 0.5V$ | 9.8 | | 8.5 | 12 | | 6.8 | | mA |
| | | $V_{DD} = 15V$, $V_O = 1.5V$ | 29 | | 25 | 40 | | 20 | | mA |
| $I_{OH}$ | High Level Output Current (Note 3) | $V_{IH} = V_{DD}$, $V_{IL} = 0V$ | | | | | | | | |
| | | $V_{DD} = 5V$, $V_O = 4.6V$ | −1.0 | | −0.9 | −1.6 | | −0.72 | | mA |
| | | $V_{DD} = 10V$, $V_O = 9.5V$ | −2.1 | | −1.9 | −3.6 | | −1.5 | | mA |
| | | $V_{DD} = 15V$, $V_O = 13.5V$ | −7.1 | | −6.2 | −12 | | −5 | | mA |
| $I_{IN}$ | Input Current | $V_{DD} = 15V$, $V_{IN} = 0V$ | −0.3 | | −0.3 | $-10^{-5}$ | | | −1.0 | μA |
| | | $V_{DD} = 15V$, $V_{IN} = 15V$ | 0.3 | | 0.3 | $10^{-5}$ | | | 1.0 | μA |

## AC Electrical Characteristics* CD4049UBM/CD4049UBC

$T_A = 25°C$, $C_L = 50$ pF, $R_L = 200k$, $t_r = t_f = 20$ ns, unless otherwise specified

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $t_{PHL}$ | Propagation Delay Time High-to-Low Level | $V_{DD} = 5V$ | | 30 | 65 | ns |
| | | $V_{DD} = 10V$ | | 20 | 40 | ns |
| | | $V_{DD} = 15V$ | | 15 | 30 | ns |
| $t_{PLH}$ | Propagation Delay Time Low-to-High Level | $V_{DD} = 5V$ | | 45 | 85 | ns |
| | | $V_{DD} = 10V$ | | 25 | 45 | ns |
| | | $V_{DD} = 15V$ | | 20 | 35 | ns |
| $t_{THL}$ | Transition Time High-to-Low Level | $V_{DD} = 5V$ | | 30 | 60 | ns |
| | | $V_{DD} = 10V$ | | 20 | 40 | ns |
| | | $V_{DD} = 15V$ | | 15 | 30 | ns |
| $t_{TLH}$ | Transition Time Low-to-High Level | $V_{DD} = 5V$ | | 60 | 120 | ns |
| | | $V_{DD} = 10V$ | | 30 | 55 | ns |
| | | $V_{DD} = 15V$ | | 25 | 45 | ns |
| $C_{IN}$ | Input Capacitance | Any Input | | 15 | 22.5 | pF |

*AC Parameters are guaranteed by DC correlated testing.

## AC Electrical Characteristics* CD4050BM/CD4050BC

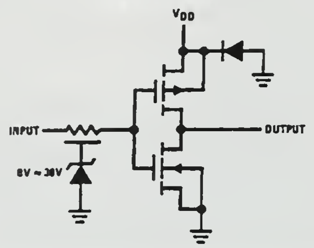
$T_A = 25°C$, $C_L = 50$ pF, $R_L = 200k$, $t_r = t_f = 20$ ns, unless otherwise specified

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $t_{PHL}$ | Propagation Delay Time High-to-Low Level | $V_{DD} = 5V$ | | 60 | 110 | ns |
| | | $V_{DD} = 10V$ | | 25 | 55 | ns |
| | | $V_{DD} = 15V$ | | 20 | 30 | ns |
| $t_{PLH}$ | Propagation Delay Time Low-to-High Level | $V_{DD} = 5V$ | | 60 | 120 | ns |
| | | $V_{DD} = 10V$ | | 30 | 55 | ns |
| | | $V_{DD} = 15V$ | | 25 | 45 | ns |
| $t_{THL}$ | Transition Time High-to-Low Level | $V_{DD} = 5V$ | | 30 | 60 | ns |
| | | $V_{DD} = 10V$ | | 20 | 40 | ns |
| | | $V_{DD} = 15V$ | | 15 | 30 | ns |
| $t_{TLH}$ | Transition Time Low-to-High Level | $V_{DD} = 5V$ | | 60 | 120 | ns |
| | | $V_{DD} = 10V$ | | 30 | 55 | ns |
| | | $V_{DD} = 15V$ | | 25 | 45 | ns |
| $C_{IN}$ | Input Capacitance | Any Input | | 5 | 7.5 | pF |

*AC Parameters are guaranteed by DC correlated testing.

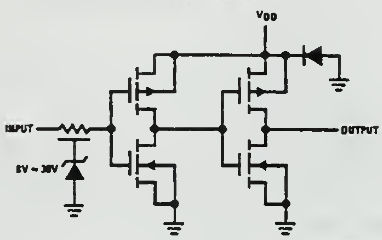
## Schematic Diagrams

**CD4049UBM/CD4049UBC**
**1 of 6 Identical Units**




TL/F/5971-3

**CD4050BM/CD4050BC**
**1 of 6 Identical Units**

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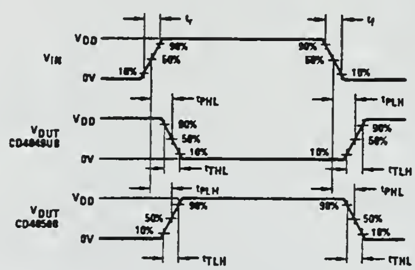
## Switching Time Waveforms

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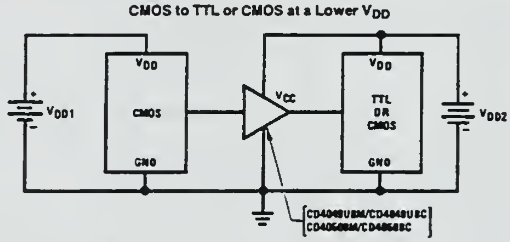
## Typical Applications

**CMOS to TTL or CMOS at a Lower $V_{DD}$**

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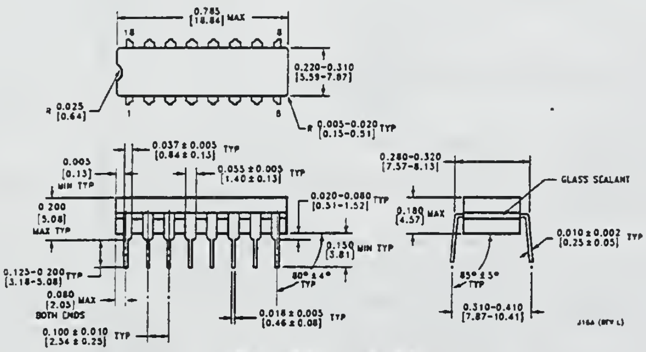
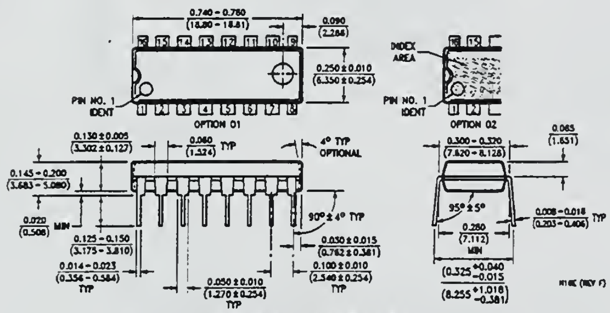
Note: $V_{DD1} \geq V_{DD2}$

Note: In the case of the CD4049UBM/CD4049UBC the output drive capability increases with increasing input voltage. E.g., if $V_{DD1}$ = 10V the CD4049UBM/CD4049UBC could drive 4 TTL loads.

## Physical Dimensions inches (millimeters)




**Ceramic Dual-In-Line Package (J)**
**Order Number CD4049UBMJ, CD4049UBCJ, CD4049BMJ or CD4049BCJ**
**NS Package Number J16A**




**Molded Dual-In-Line Package (N)**
**Order Number CD4050BMN, CD4050BCN, CD4050BMN or CD4050BCN**
**NS Package Number N16E**

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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National Semiconductor

June 1992

# CD4066BM/CD4066BC Quad Bilateral Switch

## General Description

The CD4066BM/CD4066BC is a quad bilateral switch intended for the transmission or multiplexing of analog or digital signals. It is pin-for-pin compatible with CD4016BM/CD4016BC, but has a much lower "ON" resistance, and "ON" resistance is relatively constant over the input-signal range.

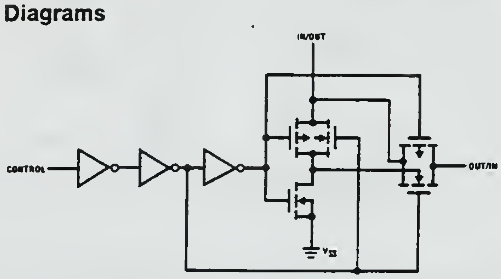
## Features

- Wide supply voltage range — 3V to 15V
- High noise immunity — 0.45 $V_{DD}$ (typ.)
- Wide range of digital and analog switching — $\pm 7.5$ $V_{PEAK}$
- "ON" resistance for 15V operation — 80Ω
- Matched "ON" resistance over 15V signal input — $\Delta R_{ON} = 5\Omega$ (typ.)
- "ON" resistance flat over peak-to-peak signal range
- High "ON"/"OFF" output voltage ratio — 65 dB (typ.) @ $f_{is} = 10$ kHz, $R_L = 10$ kΩ
- High degree linearity — 0.1% distortion (typ.)
  High degree linearity — @ $f_{is} = 1$ kHz, $V_{is} = 5V_{p-p}$,
  High degree linearity — $V_{DD} - V_{SS} = 10V$, $R_L = 10$ kΩ
- Extremely low "OFF" switch leakage — 0.1 nA (typ.) @ $V_{DD} - V_{SS} = 10V$, $T_A = 25°C$
- Extremely high control input impedance — $10^{12}\Omega$ (typ.)
- Low crosstalk between switches — $-50$ dB (typ.) @ $f_{is} = 0.9$ MHz, $R_L = 1$ kΩ
- Frequency response, switch "ON" — 40 MHz (typ.)

## Applications

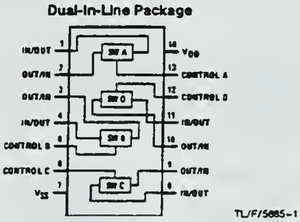
- Analog signal switching/multiplexing
  - Signal gating
  - Squelch control
  - Chopper
  - Modulator/Demodulator
  - Commutating switch
- Digital signal switching/multiplexing
- CMOS logic implementation
- Analog-to-digital/digital-to-analog conversion
- Digital control of frequency, impedance, phase, and analog-signal-gain

## Schematic and Connection Diagrams




Order Number CD4066B

Dual-In-Line Package




Top View

TL/F/5665-1



RRD-B30M105/Printed in U. S. A.

## Absolute Maximum Ratings (Notes 1 & 2)

**If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.**

| | |
|---|---|
| Supply Voltage ($V_{DD}$) | −0.5V to +18V |
| Input Voltage ($V_{IN}$) | −0.5V to $V_{DD}$ +0.5V |
| Storage Temperature Range ($T_S$) | −65°C to +150°C |
| Power Dissipation ($P_D$) | |
| Dual-In-Line | 700 mW |
| Small Outline | 500 mW |
| Lead Temperature ($T_L$) (Soldering, 10 seconds) | 300°C |

## Recommended Operating Conditions (Note 2)

| | |
|---|---|
| Supply Voltage ($V_{DD}$) | 3V to 15V |
| Input Voltage ($V_{IN}$) | 0V to $V_{DD}$ |
| Operating Temperature Range ($T_A$) | |
| CD4066BM | −55°C to +125°C |
| CD4066BC | −40°C to +85°C |

## DC Electrical Characteristics CD4066BM (Note 2)

| Symbol | Parameter | Conditions | −55°C | | +25°C | | | +125°C | | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Typ | Max | Min | Max | |
| $I_{DD}$ | Quiescent Device Current | $V_{DD}$ = 5V<br>$V_{DD}$ = 10V<br>$V_{DD}$ = 15V | | 0.25<br>0.5<br>1.0 | | 0.01<br>0.01<br>0.01 | 0.25<br>0.5<br>1.0 | | 7.5<br>15<br>30 | μA<br>μA<br>μA |
| **SIGNAL INPUTS AND OUTPUTS** | | | | | | | | | | |
| $R_{ON}$ | "ON" Resistance | $R_L = 10\ k\Omega$ to $\frac{V_{DD}-V_{SS}}{2}$<br>$V_C = V_{DD}$, $V_{IS} = V_{SS}$ to $V_{DD}$<br>$V_{DD}$ = 5V<br>$V_{DD}$ = 10V<br>$V_{DD}$ = 15V | | 800<br>310<br>200 | | 270<br>120<br>80 | 1050<br>400<br>240 | | 1300<br>550<br>320 | Ω<br>Ω<br>Ω |
| $\Delta R_{ON}$ | Δ"ON" Resistance Between any 2 of 4 Switches | $R_L = 10\ k\Omega$ to $\frac{V_{DD}-V_{SS}}{2}$<br>$V_C = V_{DD}$, $V_{IS} = V_{SS}$ to $V_{DD}$<br>$V_{DD}$ = 10V<br>$V_{DD}$ = 15V | | | | 10<br>5 | | | | Ω<br>Ω |
| $I_{IS}$ | Input or Output Leakage Switch "OFF" | $V_C$ = 0<br>$V_{IS}$ = 15V and 0V,<br>$V_{OS}$ = 0V and 15V | | ±50 | | ±0.1 | ±50 | | ±500 | nA |
| **CONTROL INPUTS** | | | | | | | | | | |
| $V_{ILC}$ | Low Level Input Voltage | $V_{IS} = V_{SS}$ and $V_{DD}$<br>$V_{OS} = V_{DD}$ and $V_{SS}$<br>$I_{IS} = \pm 10\ \mu A$<br>$V_{DD}$ = 5V<br>$V_{DD}$ = 10V<br>$V_{DD}$ = 15V | | 1.5<br>3.0<br>4.0 | | 2.25<br>4.5<br>6.75 | 1.5<br>3.0<br>4.0 | | 1.5<br>3.0<br>4.0 | V<br>V<br>V |
| $V_{IHC}$ | High Level Input Voltage | $V_{DD}$ = 5V<br>$V_{DD}$ = 10V (see note 6)<br>$V_{DD}$ = 15V | 3.5<br>7.0<br>11.0 | | 3.5<br>7.0<br>11.0 | 2.75<br>5.5<br>8.25 | | 3.5<br>7.0<br>11.0 | | V<br>V<br>V |
| $I_{IN}$ | Input Current | $V_{DD} - V_{SS}$ = 15V<br>$V_{DD} \geq V_{IS} \geq V_{SS}$<br>$V_{DD} \geq V_C \geq V_{SS}$ | | ±0.1 | | $\pm 10^{-5}$ | ±0.1 | | ±1.0 | μA |

## DC Electrical Characteristics CD4066BC (Note 2)

| Symbol | Parameter | Conditions | −40°C | | +25°C | | | +85°C | | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Typ | Max | Min | Max | |
| $I_{DD}$ | Quiescent Device Current | $V_{DD}$ = 5V<br>$V_{DD}$ = 10V<br>$V_{DD}$ = 15V | | 1.0<br>2.0<br>4.0 | | 0.01<br>0.01<br>0.01 | 1.0<br>2.0<br>4.0 | | 7.5<br>15<br>30 | μA<br>μA<br>μA |

## DC Electrical Characteristics (Continued) CD4066BC (Note 2)

| Symbol | Parameter | Conditions | −40°C Min | −40°C Max | +25°C Min | +25°C Typ | +25°C Max | +85°C Min | +85°C Max | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| **SIGNAL INPUTS AND OUTPUTS** | | | | | | | | | | |
| $R_{ON}$ | "ON" Resistance | $R_L = 10\ k\Omega$ to $\frac{V_{DD}-V_{SS}}{2}$<br>$V_C = V_{DD}$, $V_{SS}$ to $V_{DD}$ | | | | | | | | |
| | | $V_{DD} = 5V$ | | 850 | | 270 | 1050 | | 1200 | Ω |
| | | $V_{DD} = 10V$ | | 330 | | 120 | 400 | | 520 | Ω |
| | | $V_{DD} = 15V$ | | 210 | | 80 | 240 | | 300 | Ω |
| $\Delta R_{ON}$ | Δ"ON" Resistance Between Any 2 of 4 Switches | $R_L = 10\ k\Omega$ to $\frac{V_{DD}-V_{SS}}{2}$<br>$V_{CC} = V_{DD}$, $V_{IS} = V_{SS}$ to $V_{DD}$ | | | | | | | | |
| | | $V_{DD} = 10V$ | | | | 10 | | | | Ω |
| | | $V_{DD} = 15V$ | | | | 5 | | | | Ω |
| $I_{IS}$ | Input or Output Leakage Switch "OFF" | $V_C = 0$ | | ±50 | | ±0.1 | ±50 | | ±200 | nA |
| **CONTROL INPUTS** | | | | | | | | | | |
| $V_{ILC}$ | Low Level Input Voltage | $V_{IS} = V_{SS}$ and $V_{DD}$<br>$V_{OS} = V_{DD}$ and $V_{SS}$<br>$I_{IS} = \pm 10\mu A$ | | | | | | | | |
| | | $V_{DD} = 5V$ | | 1.5 | | 2.25 | 1.5 | | 1.5 | V |
| | | $V_{DD} = 10V$ | | 3.0 | | 4.5 | 3.0 | | 3.0 | V |
| | | $V_{DD} = 15V$ | | 4.0 | | 6.75 | 4.0 | | 4.0 | V |
| $V_{IHC}$ | High Level Input Voltage | $V_{DD} = 5V$ | 3.5 | | 3.5 | 2.75 | | 3.5 | | V |
| | | $V_{DD} = 10V$ (See note 6) | 7.0 | | 7.0 | 5.5 | | 7.0 | | V |
| | | $V_{DD} = 15V$ | 11.0 | | 11.0 | 8.25 | | 11.0 | | V |
| $I_{IN}$ | Input Current | $V_{DD} - V_{SS} = 15V$<br>$V_{DD} \geq V_{IS} \geq V_{SS}$<br>$V_{DD} \geq V_C \geq V_{SS}$ | | ±0.3 | | $\pm 10^{-5}$ | ±0.3 | | ±1.0 | μA |

## AC Electrical Characteristics* $T_A = 25°C$, $t_r = t_f = 20$ ns and $V_{SS} = 0V$ unless otherwise noted

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $t_{PHL}$, $t_{PLH}$ | Propagation Delay Time Signal Input to Signal Output | $V_C = V_{DD}$, $C_L = 50$ pF, *(Figure 1)*<br>$R_L = 200k$ | | | | |
| | | $V_{DD} = 5V$ | | 25 | 55 | ns |
| | | $V_{DD} = 10V$ | | 15 | 35 | ns |
| | | $V_{DD} = 15V$ | | 10 | 25 | ns |
| $t_{PZH}$, $t_{PZL}$ | Propagation Delay Time Control Input to Signal Output High Impedance to Logical Level | $R_L = 1.0\ k\Omega$, $C_L = 50$ pF, *(Figures 2 and 3)* | | | | |
| | | $V_{DD} = 5V$ | | | 125 | ns |
| | | $V_{DD} = 10V$ | | | 60 | ns |
| | | $V_{DD} = 15V$ | | | 50 | ns |
| $t_{PHZ}$, $t_{PLZ}$ | Propagation Delay Time Control Input to Signal Output Logical Level to High Impedance | $R_L = 1.0\ k\Omega$, $C_L = 50$ pF, *(Figures 2 and 3)* | | | | |
| | | $V_{DD} = 5V$ | | | 125 | ns |
| | | $V_{DD} = 10V$ | | | 60 | ns |
| | | $V_{DD} = 15V$ | | | 50 | ns |
| | Sine Wave Distortion | $V_C = V_{DD} = 5V$, $V_{SS} = -5V$<br>$R_L = 10\ k\Omega$, $V_{IS} = 5V_{p\text{-}p}$, $f = 1$ kHz, *(Figure 4)* | | 0.1 | | % |
| | Frequency Response-Switch "ON" (Frequency at −3 dB) | $V_C = V_{DD} = 5V$, $V_{SS} = -5V$,<br>$R_L = 1\ k\Omega$, $V_{IS} = 5V_{p\text{-}p}$,<br>$20\ Log_{10}\ V_{OS}/V_{OS}$ (1 kHz) − dB, *(Figure 4)* | | 40 | | MHz |

## AC Electrical Characteristics* (Continued) $T_A = 25°C$, $t_r = t_f = 20$ ns and $V_{SS} = 0V$ unless otherwise noted

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| | Feedthrough — Switch "OFF" (Frequency at −50 dB) | $V_{DD} = 5.0V$, $V_{CC} = V_{SS} = -5.0V$, $R_L = 1\ k\Omega$, $V_{IS} = 5.0V_{p\text{-}p}$, 20 $Log_{10}$, $V_{OS}/V_{IS} = -50$ dB, *(Figure 4)* | | 1.25 | | |
| | Crosstalk Between Any Two Switches (Frequency at −50 dB) | $V_{DD} = V_{C(A)} = 5.0V$; $V_{SS} = V_{C(B)} = 5.0V$, $R_L 1\ k\Omega$, $V_{IS(A)} = 5.0\ V_{p\text{-}p}$, 20 $Log_{10}$, $V_{OS(B)}/V_{IS(A)} = -50$ dB *(Figure 5)* | | 0.9 | | MHz |
| | Crosstalk; Control Input to Signal Output | $V_{DD} = 10V$, $R_L = 10\ k\Omega$, $R_{IN} = 1.0\ k\Omega$, $V_{CC} = 10V$ Square Wave, $C_L = 50$ pF *(Figure 6)* | | 150 | | $mV_{p\text{-}p}$ |
| | Maximum Control Input | $R_L = 1.0\ k\Omega$, $C_L = 50$ pF, *(Figure 7)* $V_{OS(f)} = \frac{1}{2} V_{OS}(1.0\ kHz)$ | | | | |
| | | $V_{DD} = 5.0V$ | | 6.0 | | MHz |
| | | $V_{DD} = 10V$ | | 8.0 | | MHz |
| | | $V_{DD} = 15V$ | | 8.5 | | MHz |
| $C_{IS}$ | Signal Input Capacitance | | | 8.0 | | pF |
| $C_{OS}$ | Signal Output Capacitance | $V_{DD} = 10V$ | | 8.0 | | pF |
| $C_{IOS}$ | Feedthrough Capacitance | $V_C = 0V$ | | 0.5 | | pF |
| $C_{IN}$ | Control Input Capacitance | | | 5.0 | 7.5 | pF |

*AC Parameters are guaranteed by DC correlated testing.

**Note 1:** "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.

**Note 2:** $V_{SS} = 0V$ unless otherwise specified.

**Note 3:** These devices should not be connected to circuits with the power "ON".

**Note 4:** In all cases, there is approximately 5 pF of probe and jig capacitance in the output; however, this capacitance is included in $C_L$ wherever it is specified.

**Note 5:** $V_{IS}$ is the voltage at the in/out pin and $V_{OS}$ is the voltage at the out/in pin. $V_C$ is the voltage at the control input.

**Note 6:** Conditions for $V_{IHC}$: a) $V_{IS} = V_{DD}$, $I_{OS}$ = standard B series $I_{OH}$ b) $V_{IS} = 0V$, $I_{OL}$ = standard B series $I_{OL}$.

## AC Test Circuits and Switching Time Waveforms

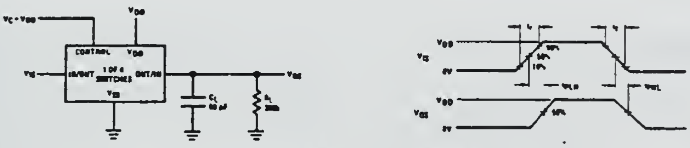


FIGURE 1. $t_{PHL}$, $t_{PLH}$ Propagation Delay Time Signal Input to Signal Output

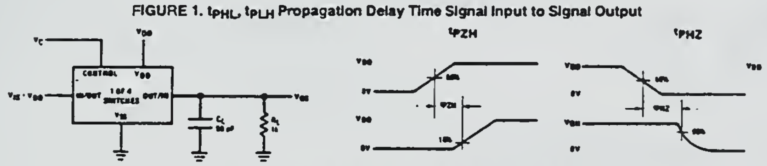
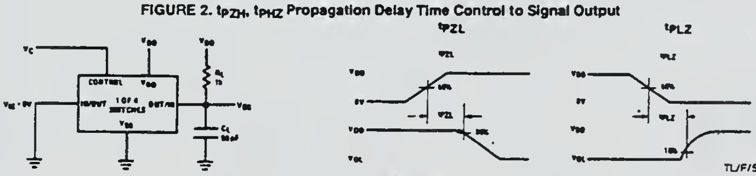



FIGURE 2. $t_{PZH}$, $t_{PHZ}$ Propagation Delay Time Control to Signal Output




TL/F/5665-2

FIGURE 3. $t_{PZL}$, $t_{PLZ}$ Propagtion Delay Time Control to Signal Output

## AC Test Circuits and Switching Time Waveforms (Continued)

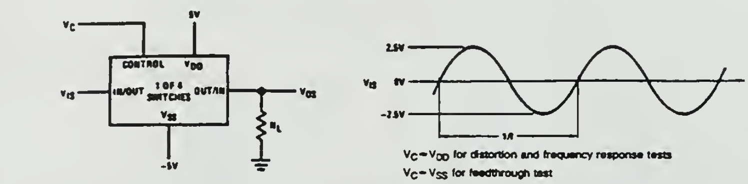



FIGURE 4. Sine Wave Distortion, Frequency Response and Feedthrough

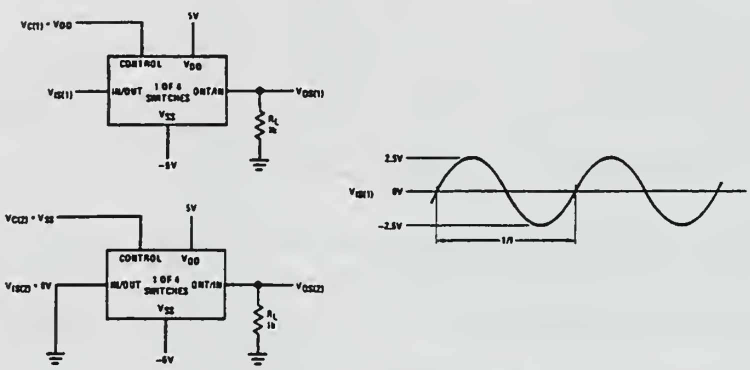



FIGURE 5. Crosstalk Between Any Two Switches

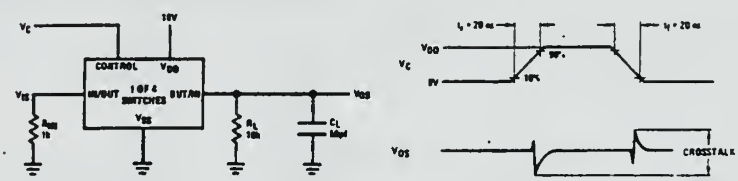
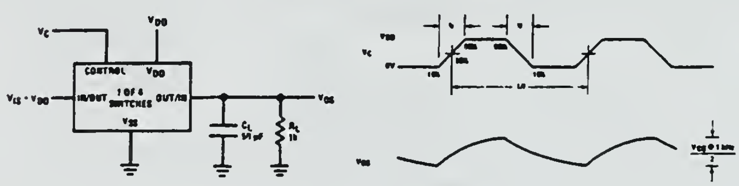



FIGURE 6. Crosstalk: Control Input to Signal Output

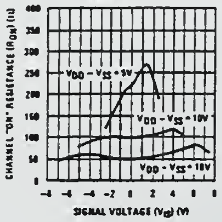



TL/F/5665-3

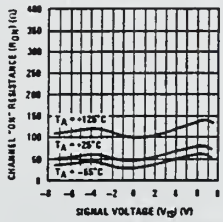
FIGURE 7. Maximum Control Input Frequency

## Typical Performance Characteristics

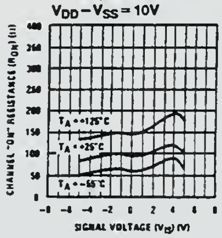
"ON" Resistance vs Signal Voltage for $T_A = 25°C$



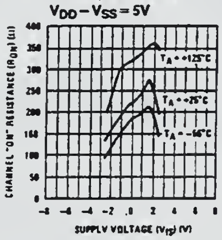

"ON" Resistance as a Function of Temperature for $V_{DD} - V_{SS} = 15V$




"ON" Resistance as a Function of Temperature for $V_{DD} - V_{SS} = 10V$




"ON" Resistance as a Function of Temperature for $V_{DD} - V_{SS} = 5V$




TL/F/5665–4

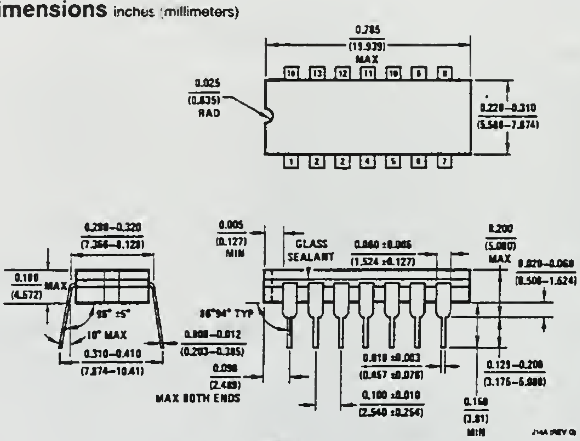
## Special Considerations

In applications where separate power sources are used to drive $V_{DD}$ and the signal input, the $V_{DD}$ current capability should exceed $V_{DD}/R_L$ ($R_L$ = effective external load of the 4 CD4066BM/CD4066BC bilateral switches). This provision avoids any permanent current flow or clamp action of the $V_{DD}$ supply when power is applied or removed from CD4066BM/CD4066BC.

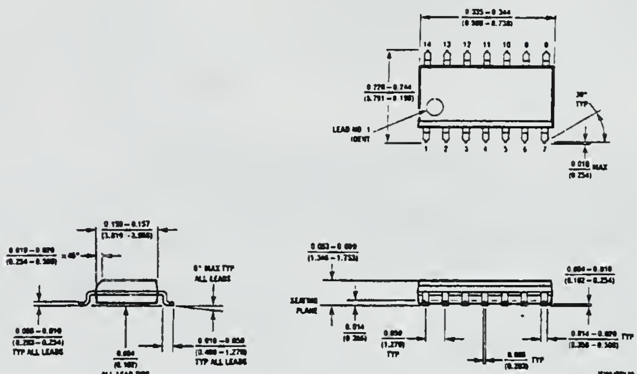
In certain applications, the external load-resistor current may include both $V_{DD}$ and signal-line components. To avoid drawing $V_{DD}$ current when switch current flows into terminals 1, 4, 8 or 11, the voltage drop across the bidirectional switch must not exceed 0.6V at $T_A \leq 25°C$, or 0.4V at $T_A > 25°C$ (calculated from $R_{ON}$ values shown).

No $V_{DD}$ current will flow through $R_L$ if the switch current flows into terminals 2, 3, 9 or 10.

## Physical Dimensions inches (millimeters)

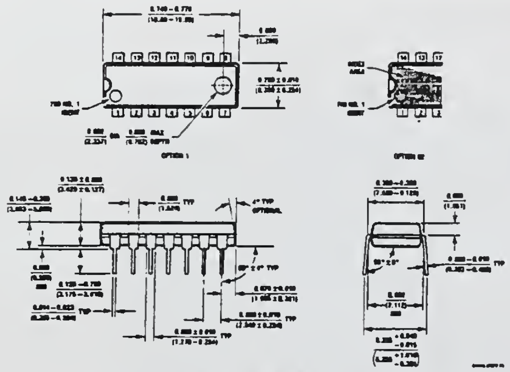



Cerdip (J)
Order Number CD4066BMJ or CD4066BCJ
NS Package Number J14A



S.O. Package (M)
Order Number CD4066BCM
NS Package Number M14A

## Physical Dimensions inches (millimeters) (Continued)



**Dual-In-Line Package (N)**
**Order Number CD4066BMN or CD4066BCN**
**NS Package Number N14A**

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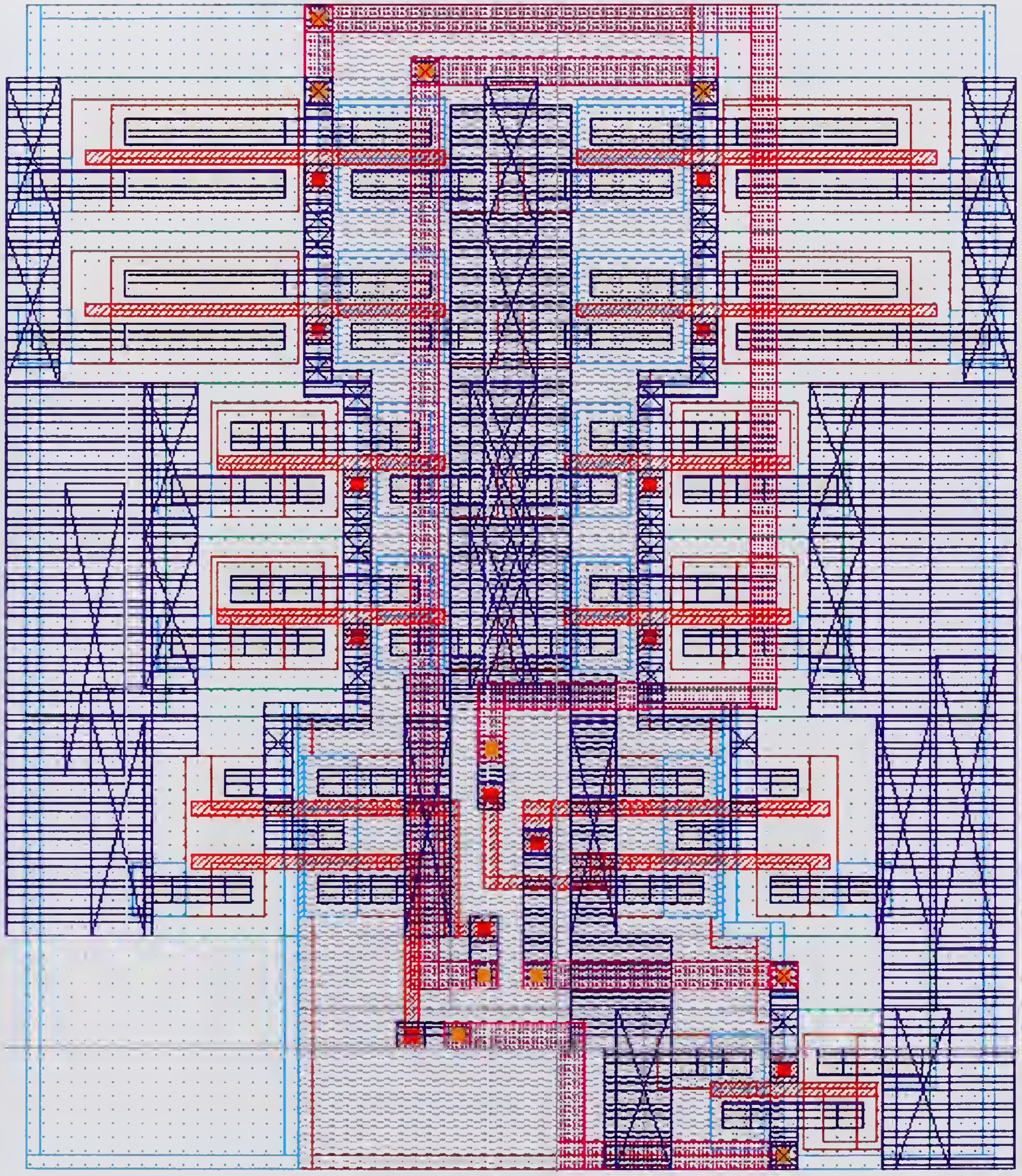
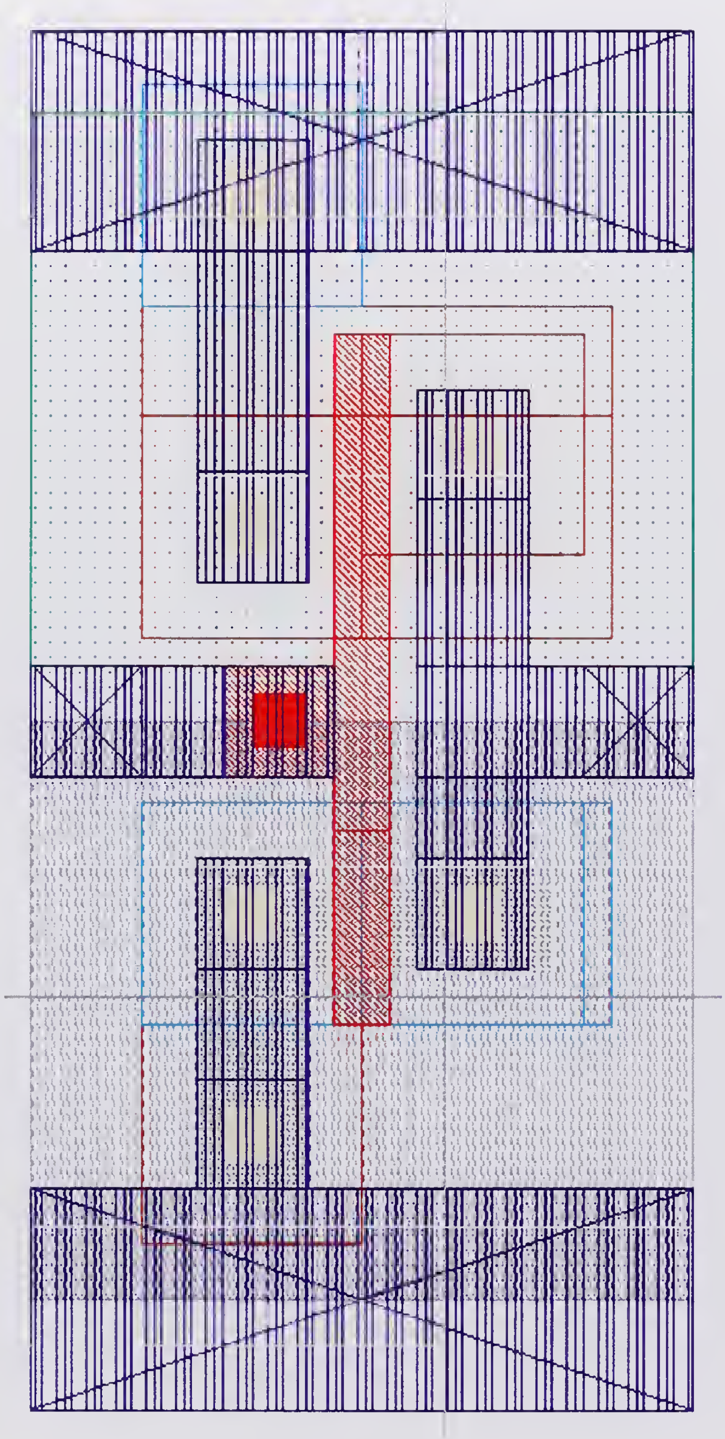
# APPENDIX B. PROGRAMMABLE GIC FILTER LAYOUT

## A. TWO PHASE CLOCK

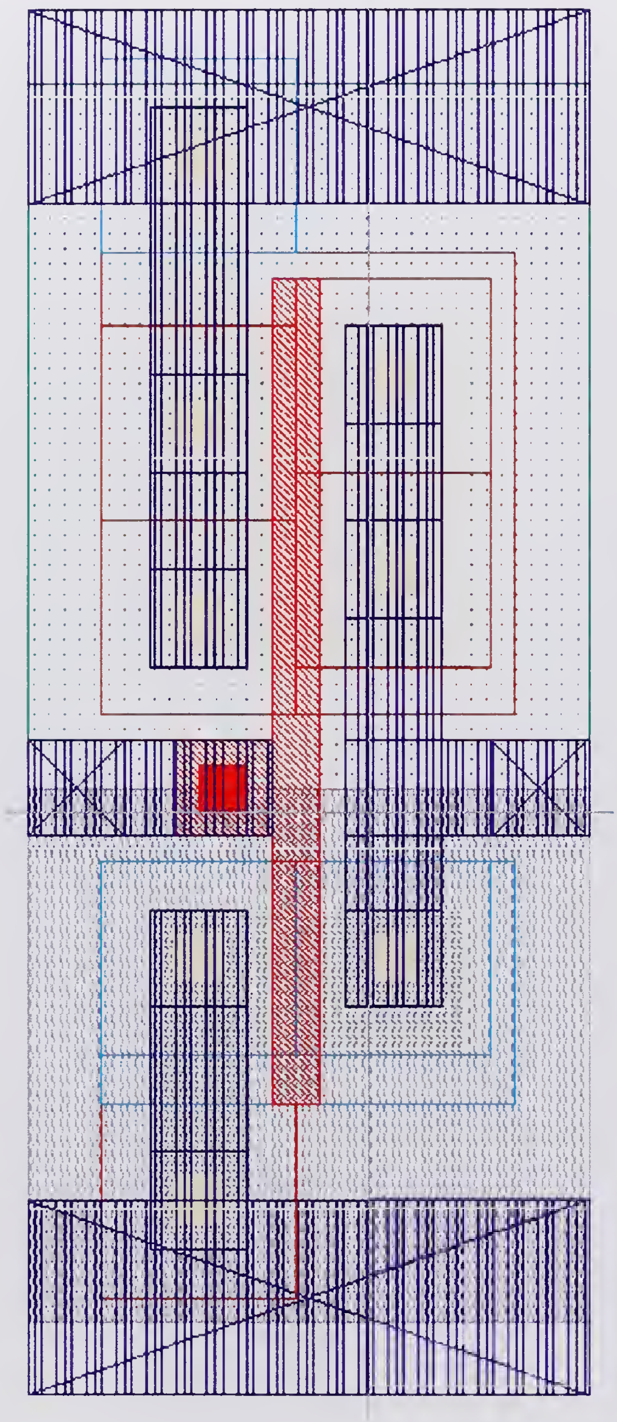
### 1. Two Phase Clock Layout



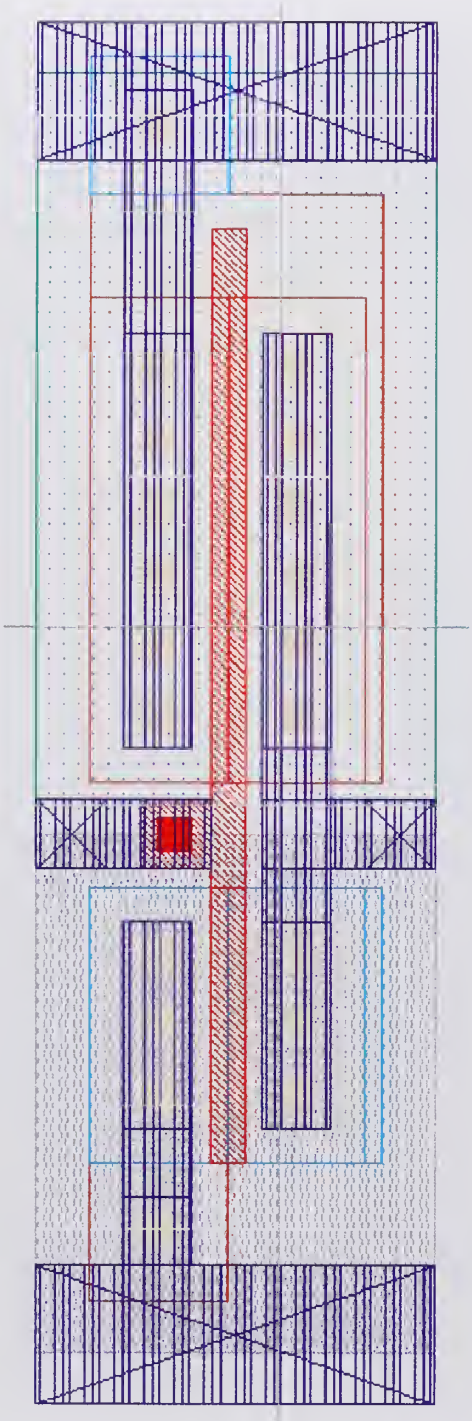
### 2. Two Phase Clock Inverter One Layout



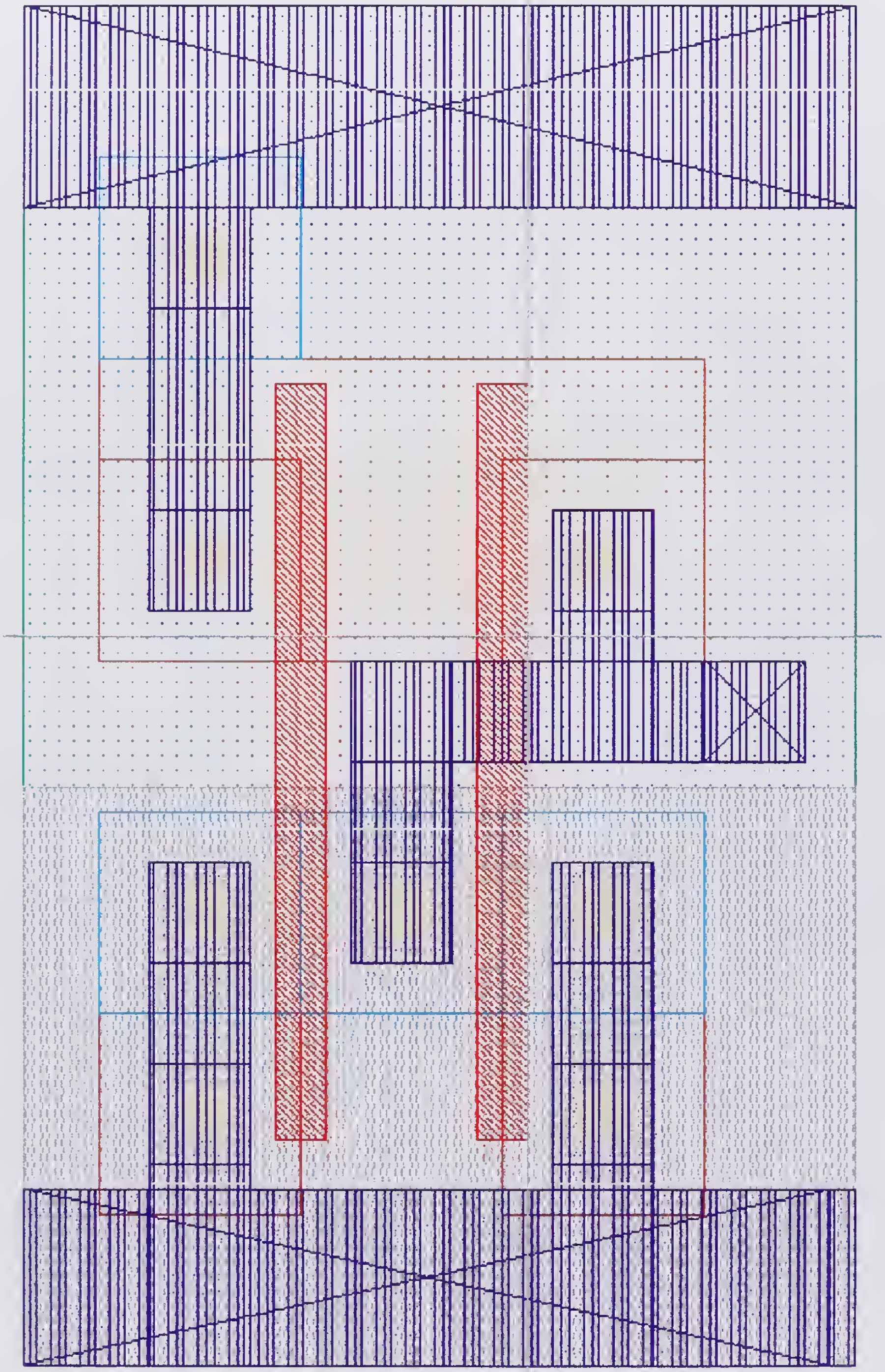
### 3. Two Phase Clock Inverter Two Layout



#### 4. Two Phase Clock Inverter Three Layout

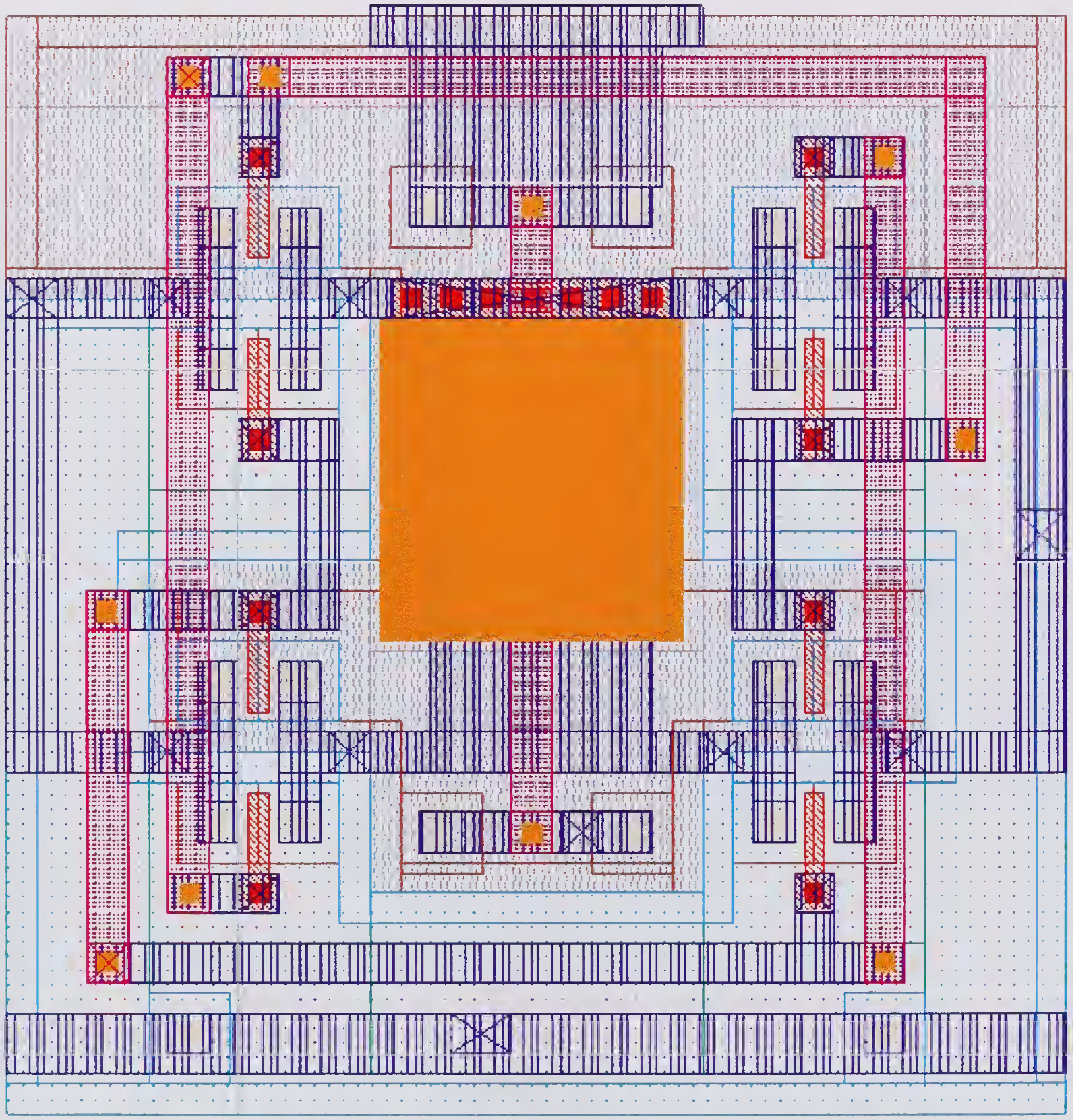


### 5. Two Phase Clock Nor Gate Layout

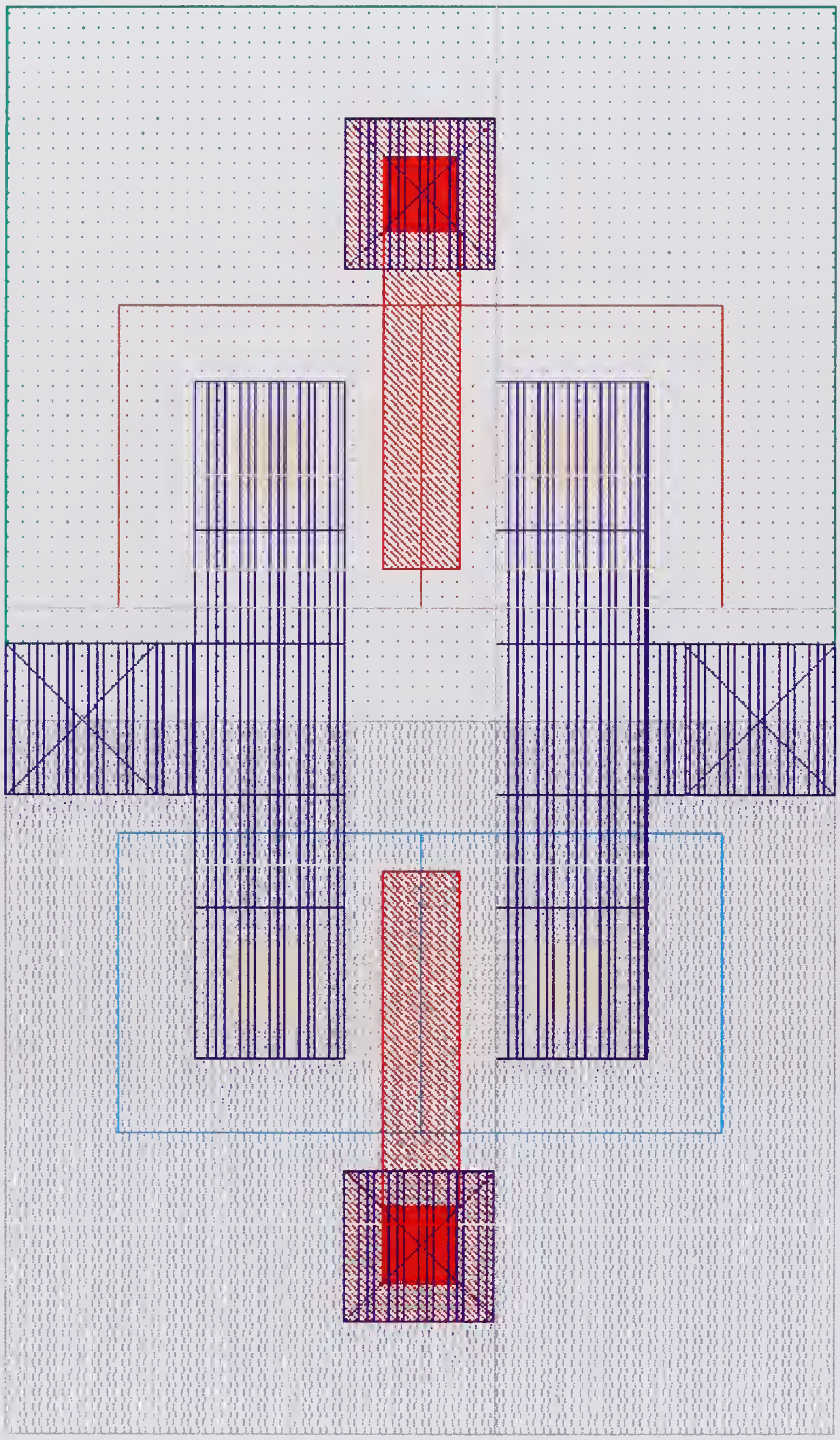


## B. BILATERAL RESISTOR

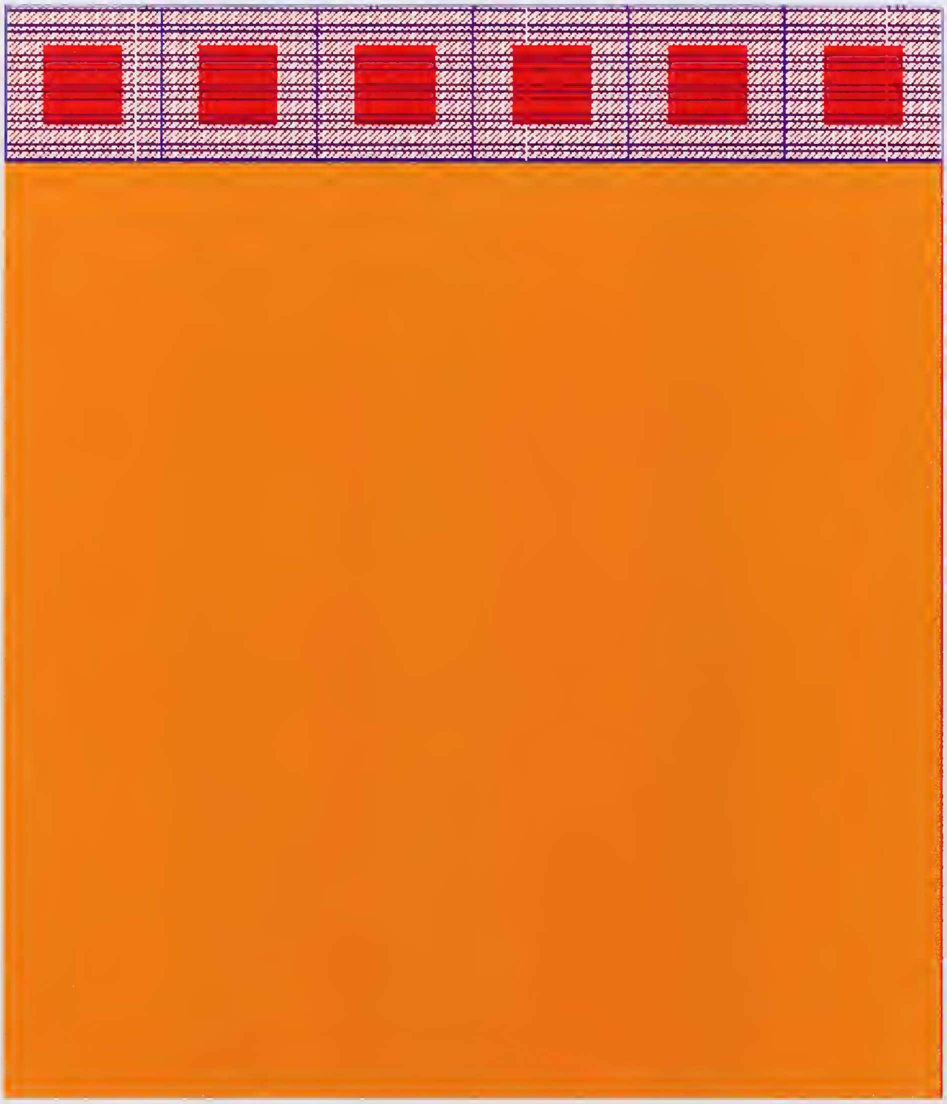
### 1. Bilateral Resistor Layout



## 2. Pass Gate Laout

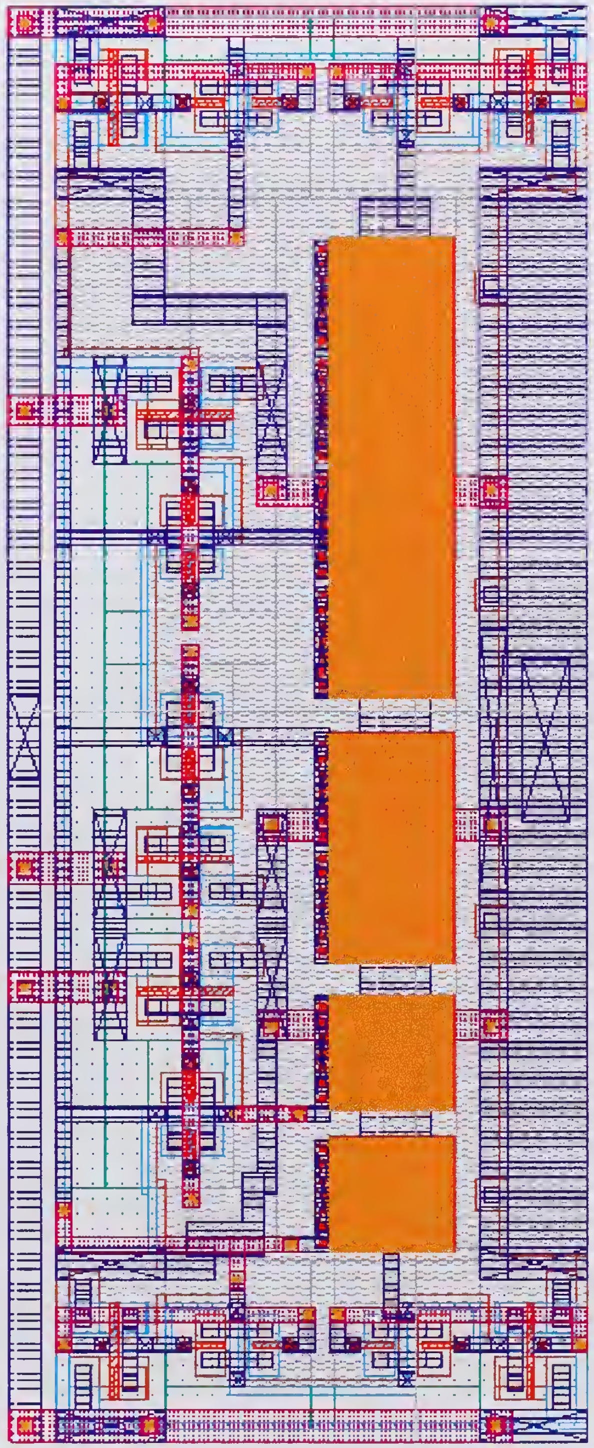


### 3. Bilateral Cap Layout

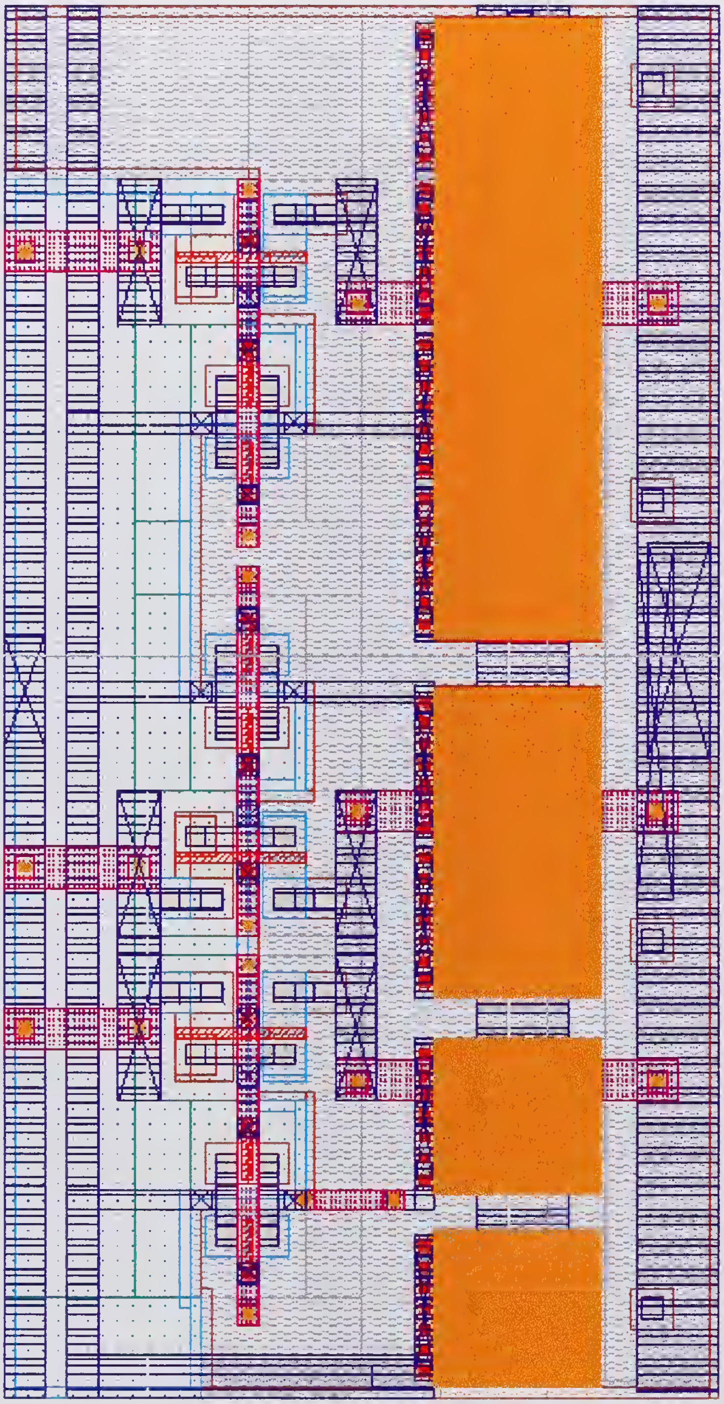


## C. VARIABLE BILATERAL ONE

### 1. Variable Bilateral One Layout

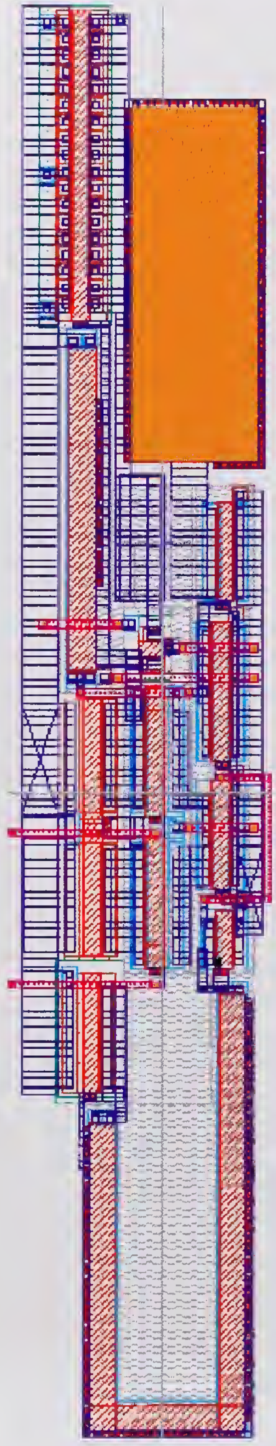


## 2. Variable Bilateral Two Layout

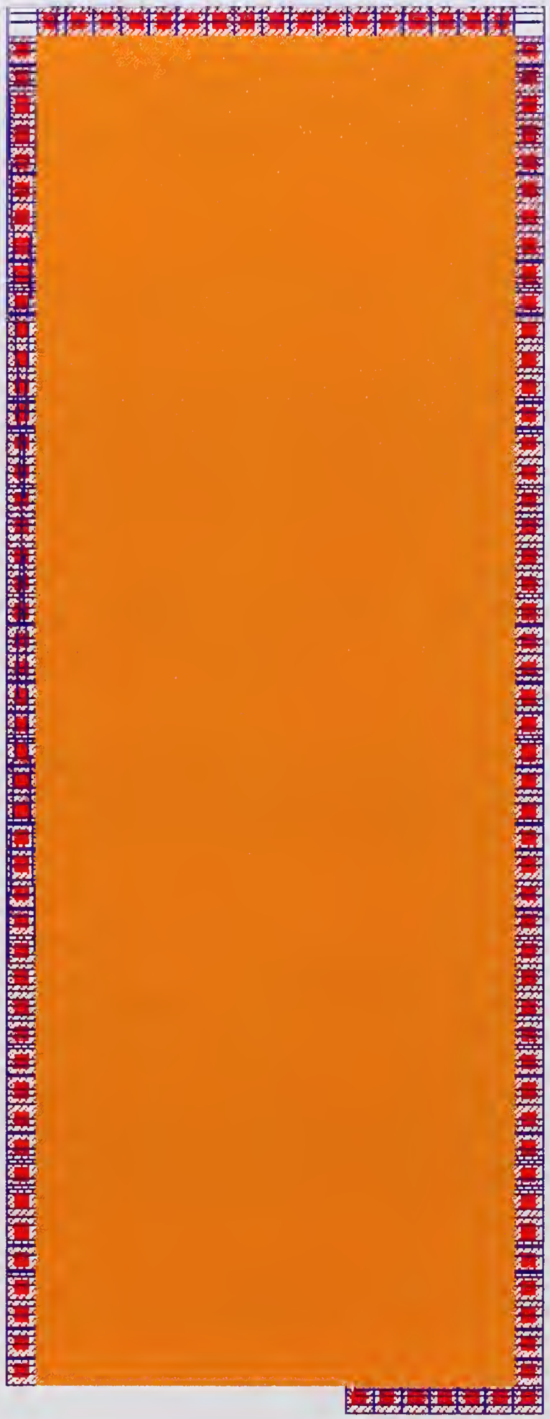


## D. OPERATIONAL AMPLIFIER

### 1. Operational Amplifier Layout

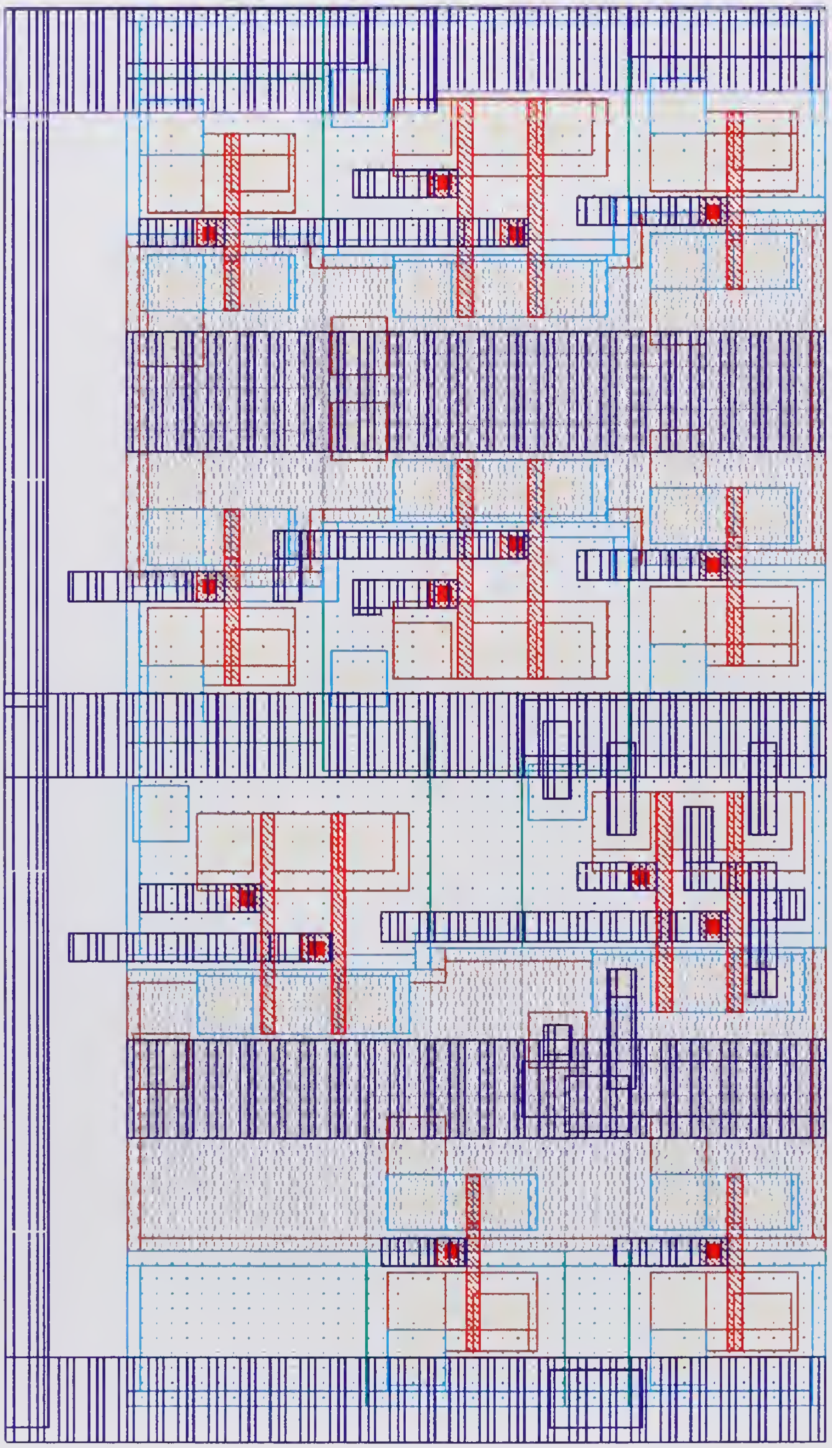


**2. 6.89pf Capacitor Layout**

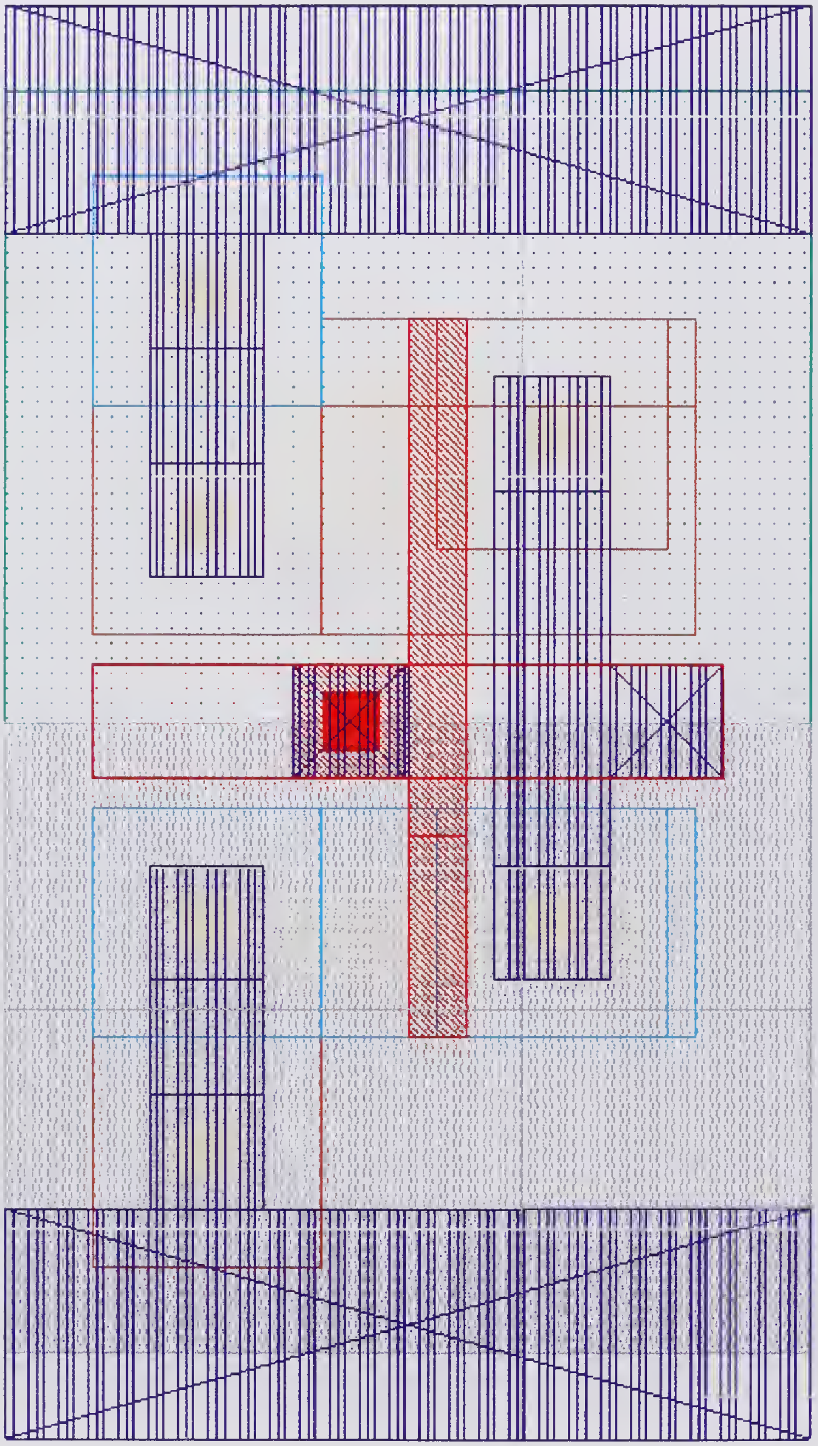


## E. FILTER LOGIC

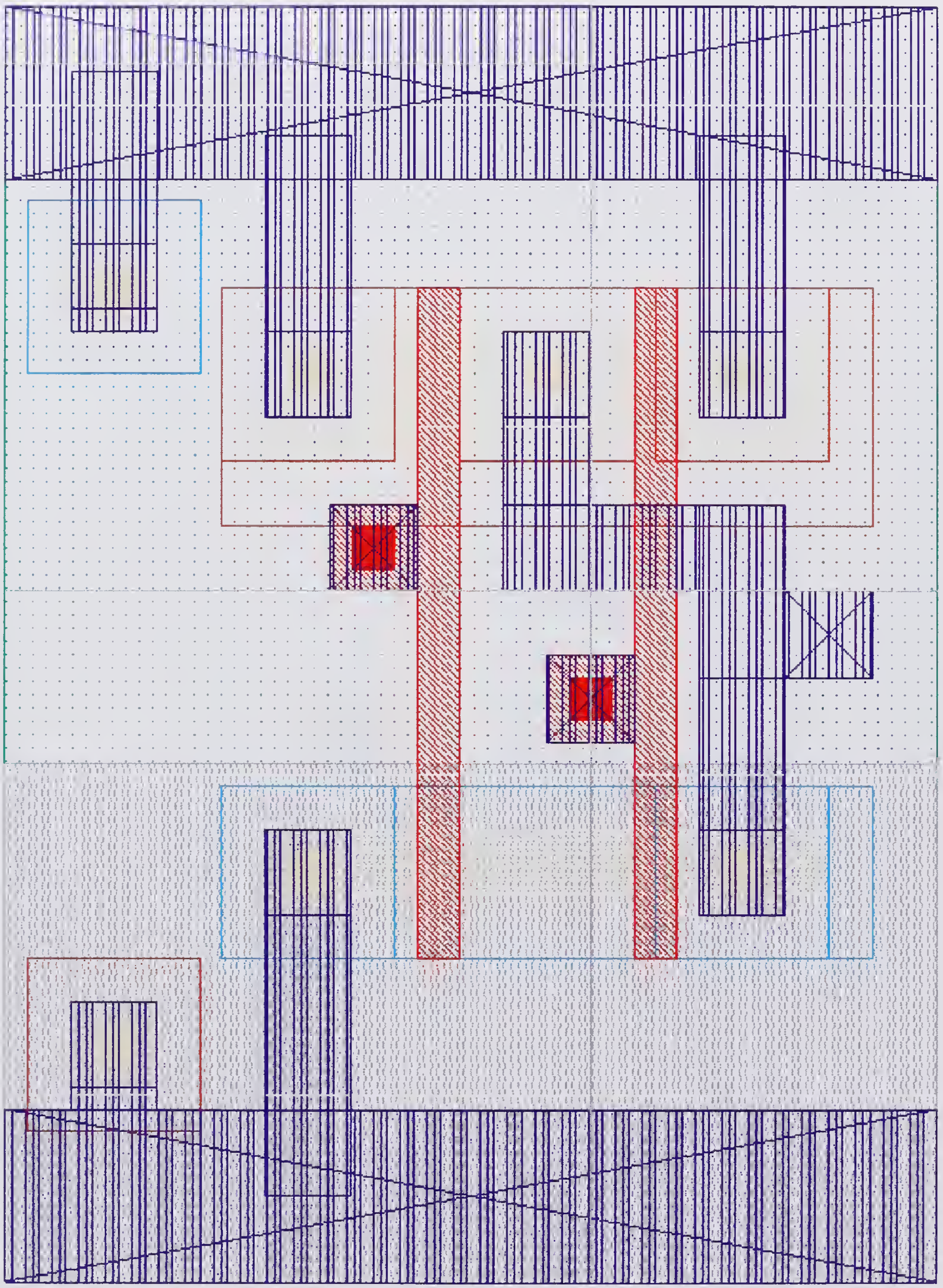
### 1. Filter Logic Layout



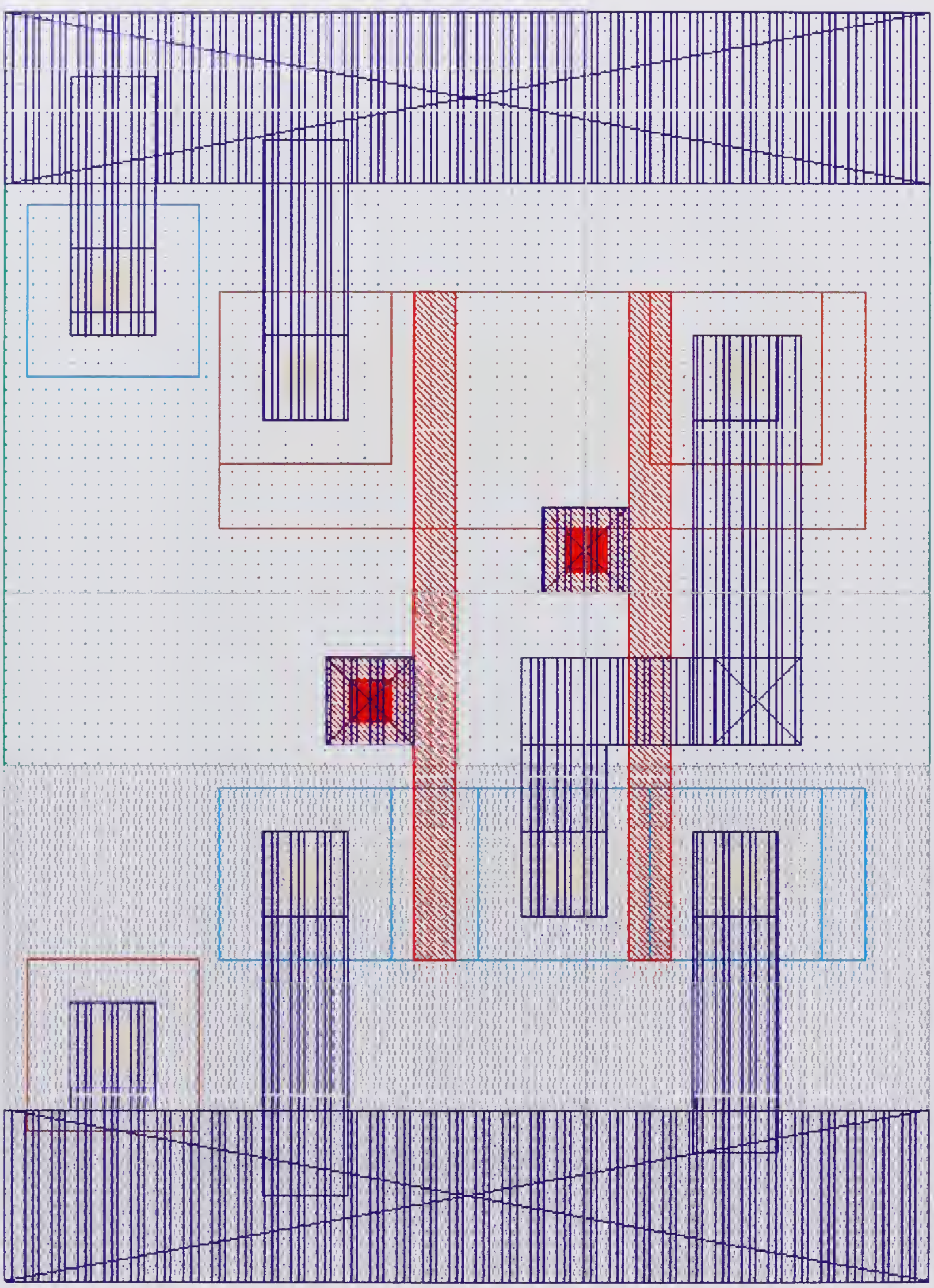
## 2. Logic Inverter Layout



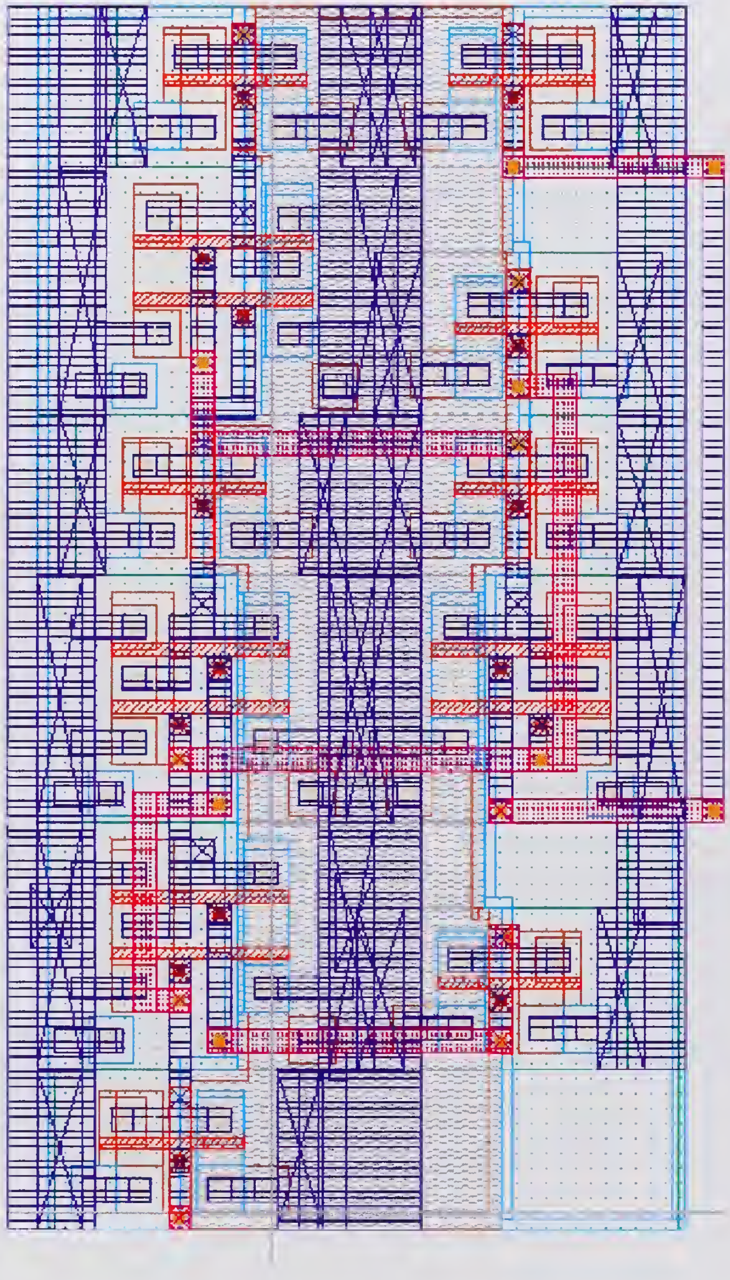
### 3. Logic NAND Gate Layout



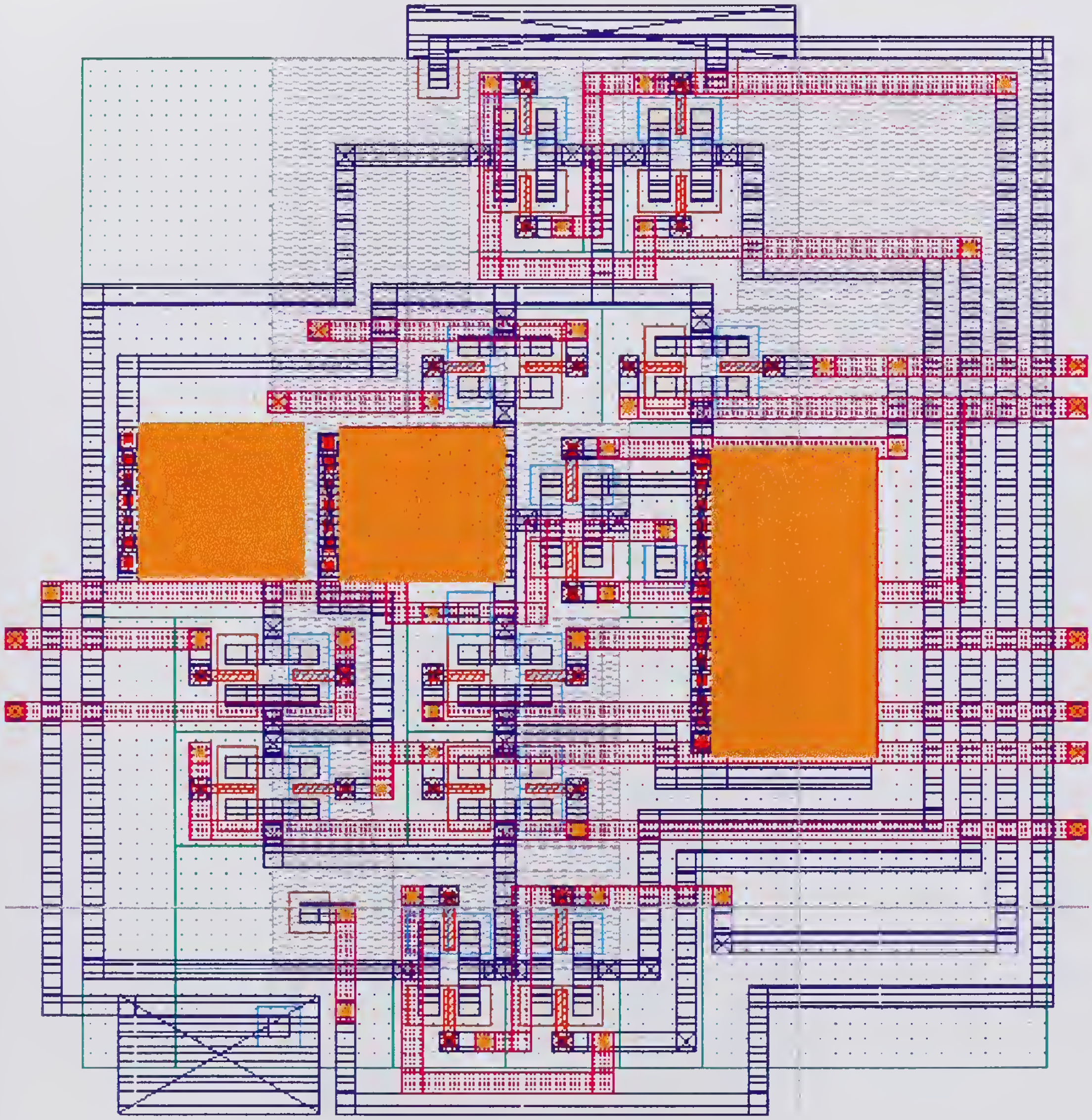
## 4. Logic NOR Gate Layout



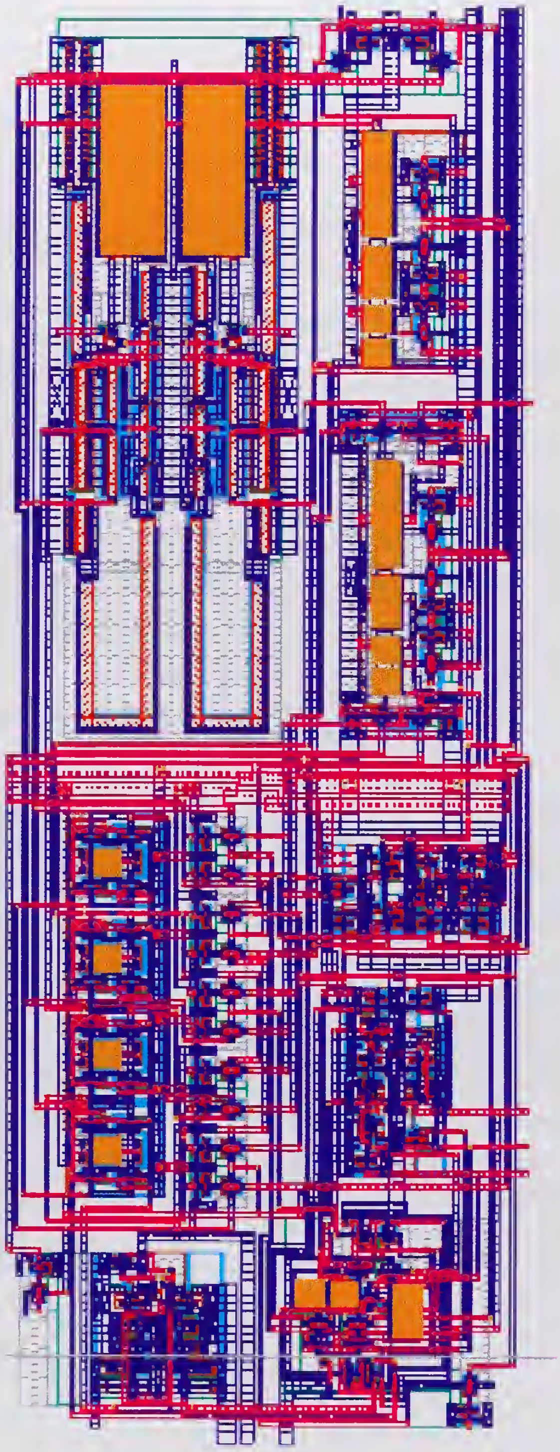
## F. FREQUENCY LOGIC LAYOUT



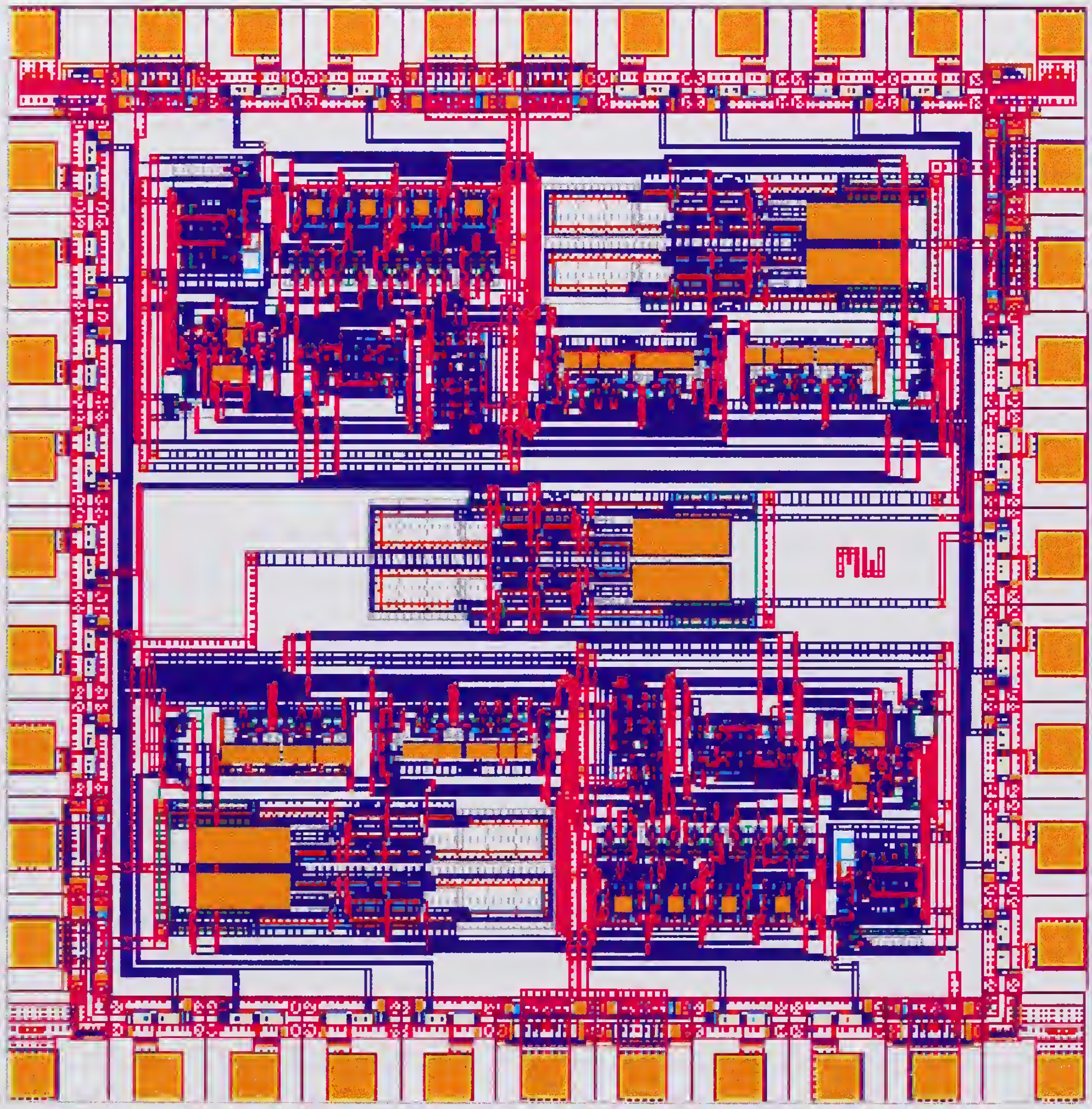
## G. QUALITY FACTOR LOGIC LAYOUT



## H. PROGRAMMABLE GIC LAYOUT



## I. PROJECT LAYOUT



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